AN1957
Application note

Microprocessor supervisor functions

Introduction

Designers of microprocessor systems have to achieve high reliability, in the face of a large number of threats to stability or even correct functioning (such as voltage drops, glitches, long ramp-up times, programs stuck in endless loops, etc.).

Supervisor circuits from STMicroelectronics provide highly effective solutions for minimizing the risks of system failure and for ensuring the safe running of the system at a low cost. The members of the ST supervisor family offer various combinations of functions.

This application note describes the main supervisor functions and features, to help the user to understand their principles and the advantages of using them, through the description of waveforms, recommended values, and hardware hookup diagrams.

Overview of ST supervisors

Microprocessor supervisors

- STM705, STM706, STM706T/S/R, STM707, STM708, STM708T/S/R, STM813L, STM706P, STM6321L/M, STM6321T/S/R, STM6821L/M, STM6821T/S/R, STM6823L/M, STM6823T/S/R, STM6824L/M, STM6824T/S/R, STM6825L/M, STM6825T/S/R

Microprocessor supervisors with switchover

- STM690A, STM692A, STM690T/S/R, STM802L/M, STM802T/S/R, STM703, STM704, STM704T/S/R, STM806T/S/R, STM805L, STM805T/S/R, STM804T/S/R, STM817L/M, STM818L/M, STM819L/M, STM795T/S/R

This application note is dedicated to the microprocessor supervisor and microprocessor supervisor with switchover families.

Contents

List of tables

List of figures

1 Overview

Table 1: Supervisor options

	3 V or 5 V supervisor	Battery switchover	Watch-dog input	Watch-dog output	Active-low $\overline{RST}$[1]	Active-high RST[1]	Manual reset input	Power-fail comparator	Chip-enable gating	Battery freshness seal
STM690T/S/R	3 V	✓	✓		✓			✓		
STM690A[2]	5 V	✓	✓		✓			✓		
STM692A[2]	5 V	✓	✓		✓			✓		
STM703[3]	5 V	✓			✓		✓	✓		
STM704[3]	5 V	✓			✓		✓	✓		
STM704T/S/R	3 V	✓			✓		✓	✓		
STM705[4]	5 V		✓	✓	✓		✓	✓		
STM706[4]	5 V		✓	✓	✓		✓	✓		
STM706T/S/R	3 V		✓	✓	✓		✓	✓		
STM706P[5]	3 V		✓	✓		✓	✓	✓		
STM707	5 V				✓	✓	✓	✓		
STM708	5 V				✓	✓	✓	✓		
STM708T/S/R	3 V				✓	✓	✓	✓		
STM795T/S/R	3 V	✓			✓[6]				✓	
STM802L/M	5 V	✓	✓		✓			✓		
STM802T/S/R	3 V	✓	✓		✓			✓		
STM804T/S/R[7]	3 V	✓	✓			✓[6]		✓		
STM805T/S/T[7]	3 V	✓	✓			✓[6]		✓		
STM805L	5 V	✓	✓			✓		✓		
STM806T/S/R	3 V	✓			✓		✓	✓		
STM813L	5 V		✓	✓		✓	✓	✓		
STM817L/M	5 V	✓	✓		✓			✓		✓
STM818L/M	5 V	✓	✓		✓				✓	✓
STM819L/M	5 V	✓			✓		✓	✓		✓

Notes:

(1) Push-pull output (unless otherwise specified).

(2) STM690A has a typical reset threshold of 4.65 V and STM692A has a typical reset threshold of 4.40 V.

(3) STM703 has a typical reset threshold of 4.65 V and STM704 has a typical reset threshold of 4.40 V.

(4) STM705 has a typical reset threshold of 4.63 V and STM706 has a typical reset threshold of 4.38 V.

(5) The STM706P is identical to the STM706R, except for its reset output which is active high.

(6) Open drain output.

(7) STM804T/S/R and STM805T/S/R have different minimum and maximum reset thresholds with V_{CC} falling and V_{CC} rising (see datasheet).

2 Power-on reset and low voltage detect

After system start-up, a certain period of time is required for the power supply voltage to stabilize. For this reason, ST supervisor devices generate a reset pulse after power-up (the minimum pulse width is t_{rec} = 140 ms, see *Table 2: "Reset timings for the STM703/704 supervisor"*). Over the t_{rec} period, during which reset is asserted, the clock is stabilized and the registers are set to their default values. This function is called power-on reset (POR).

Some designers attempt to use RC circuits, instead of a reset implementation, because it is cheaper. But it is also unsafe and unreliable. RC circuits are not suitable for use as professional devices in industrial environments (see *Section 9: "References"*, AN1772). Another major function is low voltage detect (LVD), which detects power supply brownouts and glitches. Whenever V_{CC} falls below the reset threshold (V_{RST}), the reset output is asserted and remains so t_{rec} after V_{CC} increases above the V_{rst} threshold. In the case of an RC circuit, no minimum reset pulse width is guaranteed. Also, if the triggering event is a narrow glitch, an RC circuit will only generate a poor reset, which may lead to malfunctioning of the microprocessor (failing to load registers correctly, executing invalid instructions, processing incorrect data, etc.).

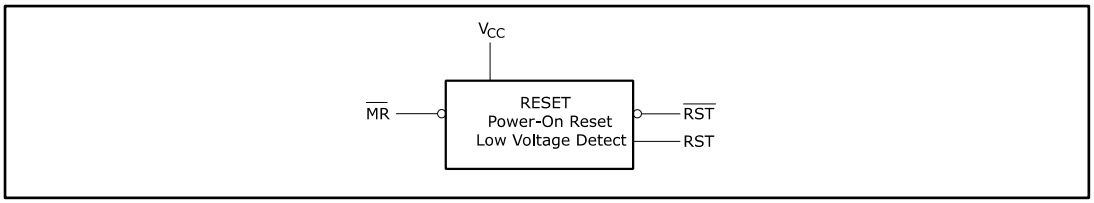
Some supervisor devices include a manual reset input ($\overline{MR}$) that can be used by the user, or the external device, to generate a reset. Typically, a low-cost push-button switch is connected to the manual reset input, which allows the user to restart the processor without turning off the power. No additional components are needed because Supervisor devices already include a debounce circuit that filters the noise of contact closure. This function can be used to debug, to perform the final test of a processor, or to restart a processor that is locked. The reset button is also useful in systems where the processor is never turned off, even when the system is in off mode. Some processors include an internal reset that operates correctly under stable power supply conditions, but usually has difficulties in handling voltage drops and transients as well as looser tolerances for V_{rst}. The use of an external reset is therefore recommended.

2.1 Block diagram showing the supervisor reset feature

Figure 1: "Supervisor reset features" illustrates the power-on reset, low-voltage detect and manual reset features. The reset is asserted if one of the following events occurs:

- System start-up
- Brownout, voltage drop, significant transient or glitch, negative voltage spike etc. on the power supply line
- Manual reset

Figure 1: Supervisor reset features



Note: V_{CC} is the supply voltage, $\overline{MR}$ is the manual reset input. $\overline{RST}$ and RST are reset outputs. Supervisor devices can have an active-low output ($\overline{RST}$), an active-high output (RST) or both.

2.2 Reset waveforms for the microprocessor supervisor devices

When the input voltage level reaches the reset threshold (V_{RST}) after system power-up, the supervisor holds the reset output signal ($\overline{RST}$) low for a minimum time of t_{rec} before driving it high again(see *Figure 2: "Power-on reset and low-voltage detect waveforms"*).

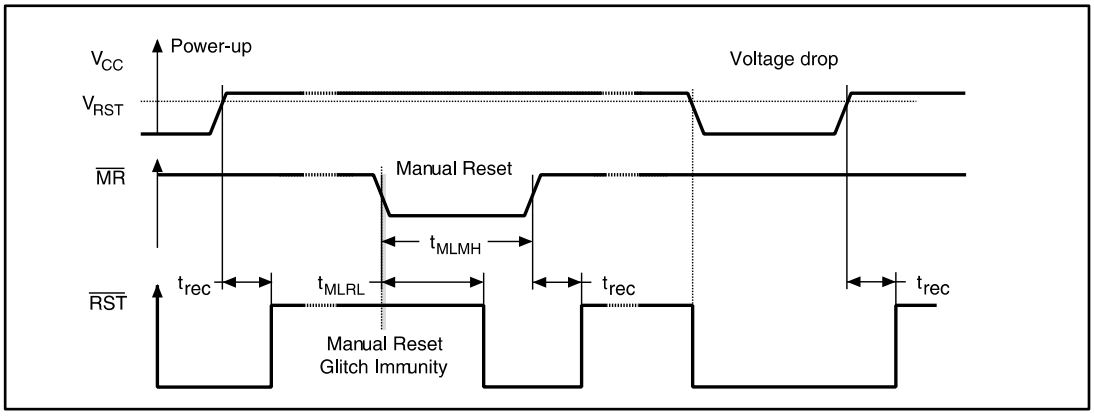
Switching the manual reset signal ($\overline{MR}$) to low, causes the $\overline{RST}$ signal to go low. $\overline{RST}$ remains low as long as $\overline{MR}$ is kept low, and returns high t_{rec} after $\overline{MR}$ has been released.

All microprocessor supervisor devices have glitch immunity. That is, the minimum $\overline{MR}$ pulse width required to reset the output is fixed. All shorter pulses are ignored.

The supervisor also reacts to voltage drops, brownouts and significant glitches. If the input voltage falls below V_{RST}, the reset output is asserted.

Note that some supervisor devices have a reset output that is active high (RST). They therefore have a waveform that is the inversion of the one that is shown in *Figure 2: "Power-on reset and low-voltage detect waveforms"*.

Figure 2: Power-on reset and low-voltage detect waveforms



Note: V_{RST} is the reset threshold, see Table 3: "Reset thresholds (V_{RST})" for values.

Table 2: Reset timings for the STM703/704 supervisor

Symbol	Alt	Parameter		Value	Unit
t_{MLMH}	$t_{\overline{MR}}$	$\overline{MR}$ pulse width	Min.	150	ns
t_{MLRL}	$t_{\overline{MRD}}$	$\overline{MR}$ to $\overline{RST}$ output delay	Max.	250	ns
t_{rec}		V_{RST} to $\overline{RST}$ high and $\overline{MR}$ high to $\overline{RST}$ high	Min.	140	ms
		Manual reset glitch immunity	Typ.	100	ns

Table 3: Reset thresholds (V_{RST})

Supervisor	Reset threshold (V_{RST})			Unit
	Min.	Typ.	Max.	
STM706P/70xR	2.55	2.63	2.70	V
STM70xS	2.85	2.93	3.00	V
STM70xT	3.00	3.08	3.15	V
STM692A/704/706/708, 8xxM	4.25	4.40	4.50	V
STM690A/703/705/707, 8xxL	4.50	4.65	4.75	V

2.3 Hardware hookup for the STM703/704 supervisor

In the example of *Figure 3: "Hardware hookup for the STM703/704 supervisor"*, the reset output is asserted in three cases:

- during system power-up, until V_{CC} is stabilized (V_{CC} is greater than V_{RST}) for a duration of t_{rec}
- after a V_{CC} drop (V_{CC} falls below V_{RST})
- by pressing the manual reset push-button (the reset button should be held for at least for t_{MLMH}).

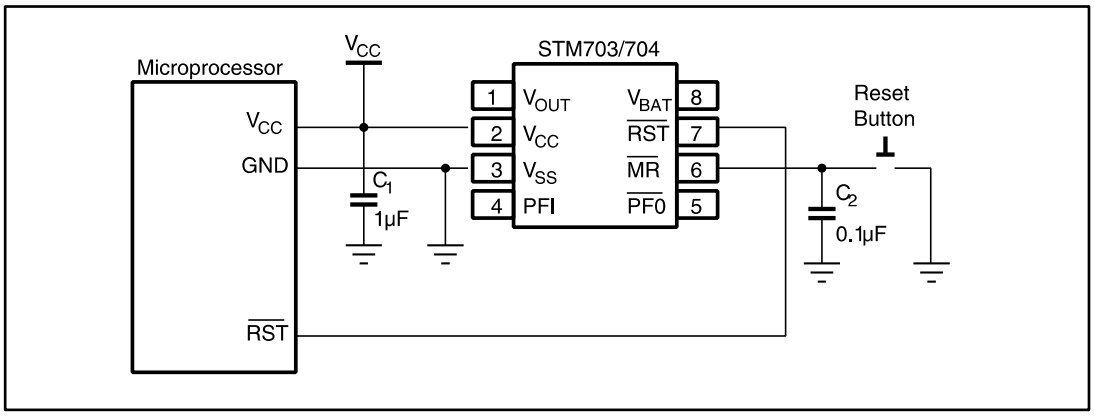
The manual reset input is not necessarily connected to a physical push button switch, it can also be connected to a peripheral, provided that a minimum $\overline{MR}$ pulse width of 150 ns is ensured.

If the reset circuit is placed in a noisy environment, or if $\overline{MR}$ is driven from long cables, it is recommended to use an external 0.1 µF capacitor, as shown in *Figure 3: "Hardware hookup for the STM703/704 supervisor"*

The $\overline{MR}$ input includes an internal pull-up resistor. So in applications where the $\overline{MR}$ input is not used, the pin can be left unconnected. The $\overline{MR}$ input can be driven with a TTL output, a CMOS output, or an open drain output.

It is always appropriate to connect a decoupling capacitor in parallel with the power supply. The recommended value is 1 µF.

Figure 3: Hardware hookup for the STM703/704 supervisor



3 Power-fail comparator

Inadvertent or unexpected power loss can cause a number of malfunctions in a system (data loss, uncontrolled program status, indeterminate processor state, etc.).

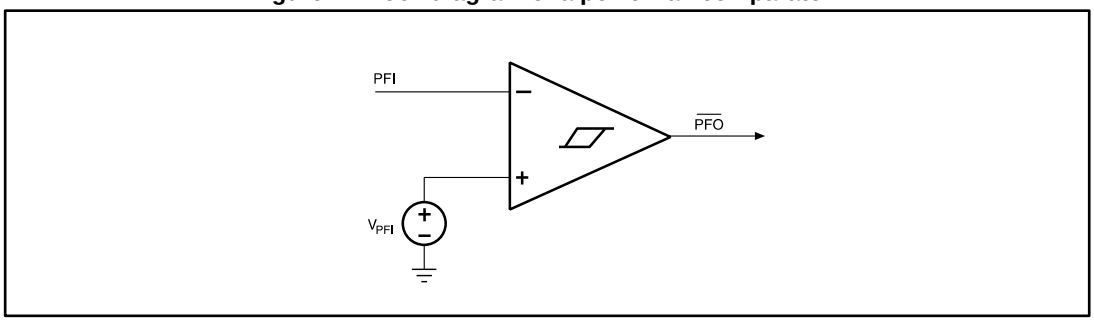
For a reliable design, systems should receive early power failure warning, to leave enough time for the microprocessor to start a safeguard routine, for backing up crucial data, registers, etc.

Power-fail comparators are used to monitor unregulated power supplies. Their reaction to power loss is very fast, and can provide enough time to execute all the necessary safeguard processes that precede an expected power failure (see *Section 9: "References"*, AN1336).

3.1 Block diagram of a power-fail comparator

The power-fail comparator works like an ordinary comparator with hysteresis (see *Figure 4: "Block diagram of a power-fail comparator"*). The power-fail input (PFI) is compared to an internal reference voltage, the power-fail threshold, V_{PFI}. If the voltage on PFI is less than V_{PFI}, the power-fail output ($\overline{PFO}$) is asserted.

Figure 4: Block diagram of a power-fail comparator



3.2 Hardware hookup for the STM692A supervisor

The power-fail comparator can be used in many different ways. It is most commonly used as an early power-fail warning (see *Figure 5: "Hardware hookup for the STM692A supervisor"*) to monitor an unregulated supply voltage.

Two external resistors R_1 and R_2 form a voltage divider to set the voltage level (V_{TRIP}) below which PFO is asserted (see the waveforms shown in *Figure 6: "Voltage drop"*).

Usually, a value is selected for R_2, then R_1 is derived using the following formula:

$$R_1 = R_2 \times \frac{V_{TRIP} - V_{PFI}}{V_{PFI}}$$

where V_{PFI} = 1.25 V.

The sum of the resistances should be about 1 MΩ to minimize power consumption, and the tolerance of the resistor should not exceed 1%, to ensure that there are not large variations in the sensed voltage.

Example calculation

We have: V_{TRIP} = 11.5 V and V_{PFI} = 1.25 V.

Let us put: R_2 = 100 kΩ

R_1 is calculated as follows:

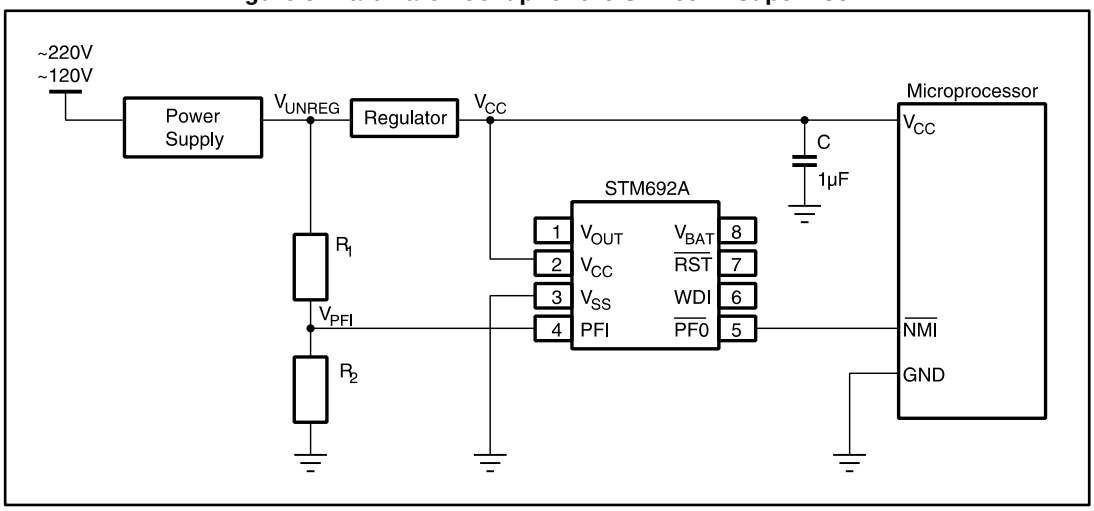
$$R_1 = R_2 \times \frac{V_{TRIP} - V_{PFI}}{V_{PFI}} = 100 \cdot 10^3 \times \frac{11.5 - 1.25}{1.25} = 820k\Omega$$

Thus R_1 = 820 kΩ.

Table 4: Recommended resistances for some V_{TRIP} voltages

V_{TRIP} (V)	R_1 (kΩ)	R_2 (kΩ)
8.5	750	130
10.0	910	130
11.5	820	100
12.5	820	91
15.0	1100	100

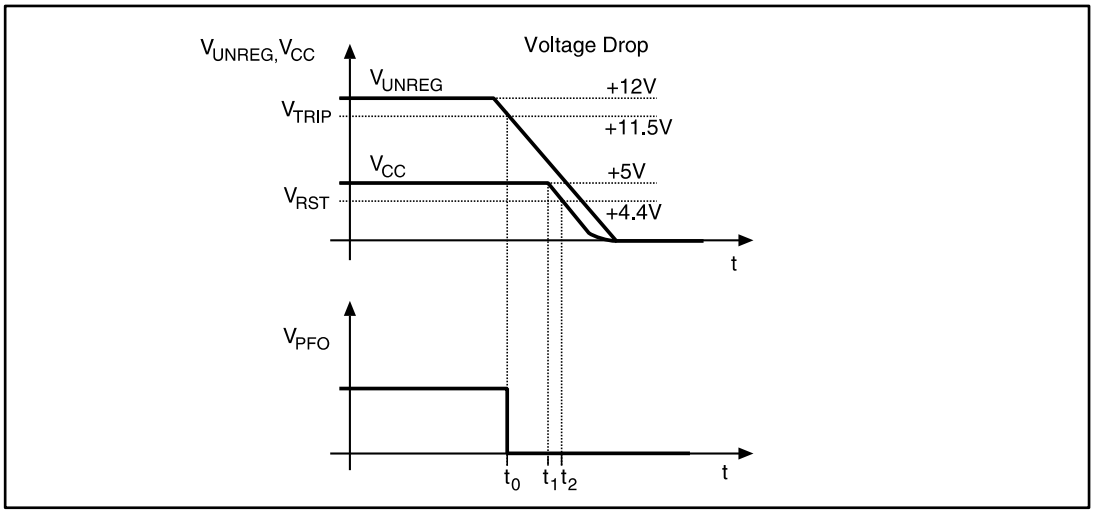
Figure 5: Hardware hookup for the STM692A supervisor



3.3 Example of power-fail waveforms

Figure 6: "Voltage drop" shows the case of a voltage drop. The unregulated power supply voltage (V_{UNREG}) begins to decrease. As it falls below V_{TRIP}, at t_0 in *Figure 6: "Voltage drop"*, $\overline{PFO}$ is asserted, invoking a non-maskable interrupt in the microprocessor, and causing the execution of the safeguard routine. The microprocessor continues operating until reset is asserted. From t_1, the power supply voltage (V_{CC}) starts to fall. At t_2 reset is asserted and write protect occurs. This means that the safeguard routine cannot last more than t_2 - t_0.

Figure 6: Voltage drop



Note: At t_0 the voltage drop is detected; at t_1 V_{CC} begins to fall; at t_2 reset is asserted and/or write protect occurs.

Table 5: Power-fail values for all microprocessor supervisors (except for STM690/704/802/804/805/806)

Symbol	Parameter		Value	Unit
V_{PFI}	Power-fail threshold	Typ.	1.25	V

Table 6: Power-fail values for 3 V microprocessor supervisors with battery switchover (STM690/704/802/804/805/806)

Symbol	Parameter		Value	Unit
V_{PFI}	Power-fail threshold	Typ.	1.237	V

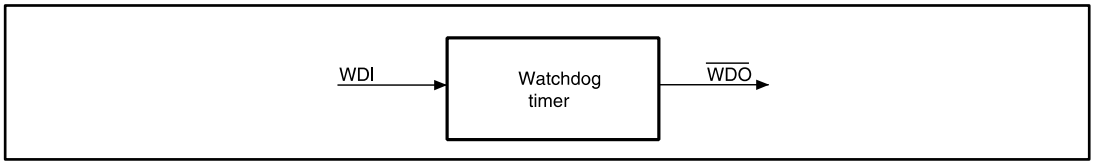
4 Watchdog timer

The role of a watchdog timer is to prevent system failures that are caused by certain types of hardware errors (non-responding peripherals, bus contention etc.) or software errors (bad code jump, code stuck in loop etc.).

The watchdog timer has an input, WDI, and an output, $\overline{WDO}$ (see *Figure 7: "Logic diagram of a watchdog timer"*). The input is used to clear the timer periodically within the specified time-out period, t_{WD} (see *Table 7: "Watchdog timer time-out value for the STM705 supervisor"*). While the system is operating correctly, it periodically toggles the watchdog input, WDI (see not found). If the system fails, the watchdog timer is not reset, and a system alert is generated: the watchdog output, $\overline{WDO}$, or the reset output, is asserted (see *Figure 8: "Watchdog timer input and output waveforms"*).

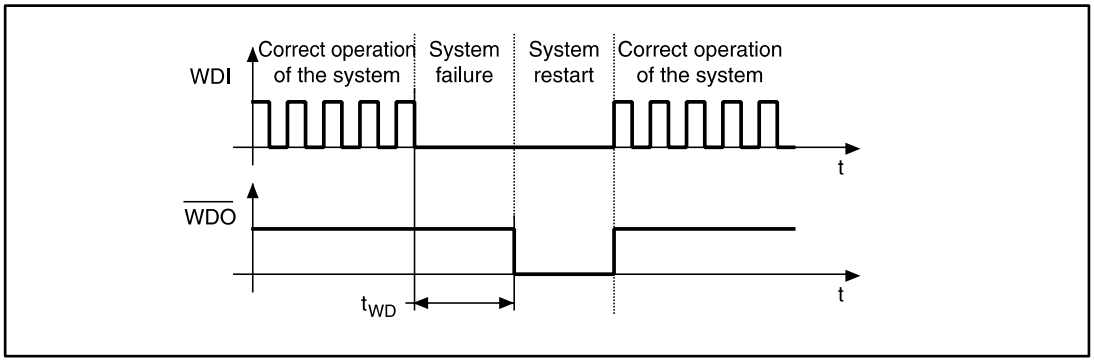
Some microprocessors have an integrated watchdog timer, with a time-out period that is software-adjustable. The great disadvantage of this solution, though, is that the integrated watchdog timer uses the same power supply, and clock signal, as the microprocessor. So, a system malfunction may also lead to a failure of the watchdog timer.

Figure 7: Logic diagram of a watchdog timer



Note: WDI is the watchdog input, $\overline{WDO}$ is the watchdog output.

Figure 8: Watchdog timer input and output waveforms



Note:

1. WDI signal frequencies greater than 50 MHz (20 ns period) will be filtered.

2. t_{WD} is the watchdog time-out period. See Table 7: "Watchdog timer time-out value for the STM705 supervisor" for value.

Table 7: Watchdog timer time-out value for the STM705 supervisor

Symbol	Description		Value	Unit
t_{WD} (1)	Watchdog time-out period	Typ.	1.6	s

Notes:

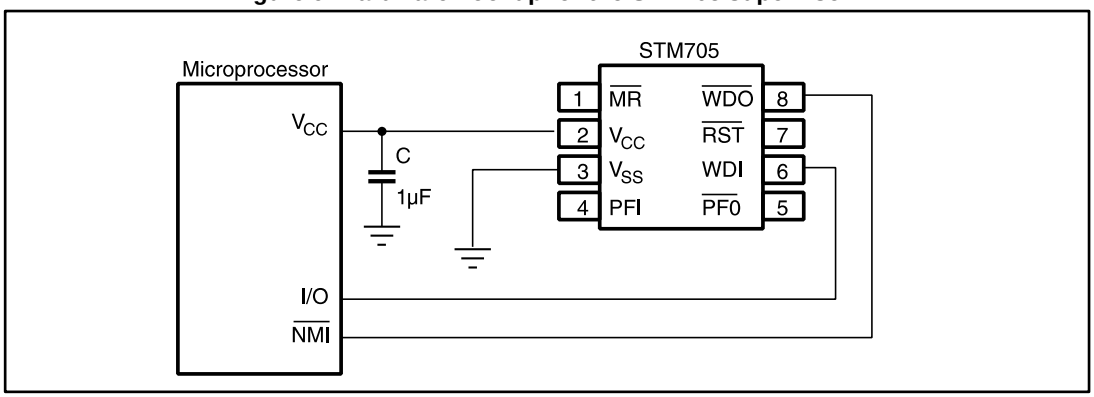
(1) This t_{WD} value is valid for all microprocessor supervisors.

4.1 Hardware hookup for the STM705 supervisor

WDI is usually connected to the output pin of the microprocessor as shown in *Figure 9: "Hardware hookup for the STM705 supervisor"* and $\overline{WDO}$ is tied to the microprocessor non-maskable interrupt ($\overline{NMI}$) or reset input.

The code should take care of clearing the watchdog timer within the time-out period by toggling the microprocessor's I/O pin.

Figure 9: Hardware hookup for the STM705 supervisor



In any case, if V_{CC} drops below the reset threshold (V_{RST}), $\overline{WDO}$ goes low even if the watchdog timer has not timed out. The timer remains cleared and does not count for as long as reset is asserted. The counter automatically restarts after t_{rec} expires.

In 5 V supply devices, the watchdog function may be disabled by floating WDI or tri-stating the driver that is connected to WDI.

5 Battery switchover

A common task of battery switchover devices is to provide an uninterrupted power supply to external devices in the event of voltage drops and brownouts.

Battery switchover devices can also be useful in portable devices. When the external power supply (such as the AC power supply adapter) is disconnected, the battery switchover device switches to the internal supply (such as a battery).

The use of a battery switchover has the following advantages:

- providing continuous and reliable service, even if the external supply fails
- extending the battery lifetime
- debouncing the power spikes occurring while connecting and disconnecting the AC adapter.

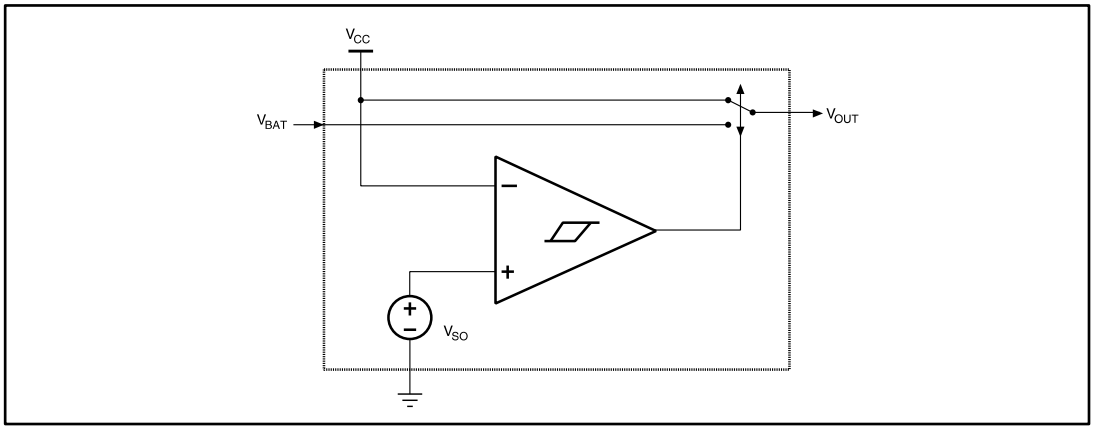
Battery switchover devices can be used as a main power supply backup for MCUs, memories and other peripherals, and to prevent system failures (see *Figure 10: "Block diagram of a battery switchover device"*).

Diode-OR connections are often used as an equivalent solution. However the diode voltage drop represents a large percentage of the battery voltage, and power supply spikes are not filtered. With an ST supervisor, the device is supplied from the main power supply as long as the voltage is high enough, even if the battery voltage is greater than the power supply voltage, which saves the battery and extends its lifetime.

Instead of a backup battery it is also possible to use a backup capacitor. Recommended capacitor values start from 0.1 F.

The battery switchover device monitors the power supply voltage, V_{CC}, which is compared to the reference voltage, V_{SO}, as shown in *Figure 11: "Battery switchover waveforms for the STM806R supervisor"* If V_{CC} drops too low, the V_{OUT} output is switched to the battery voltage, V_{BAT}. The comparator includes hysteresis for noise immunity purposes.

Figure 10: Block diagram of a battery switchover device

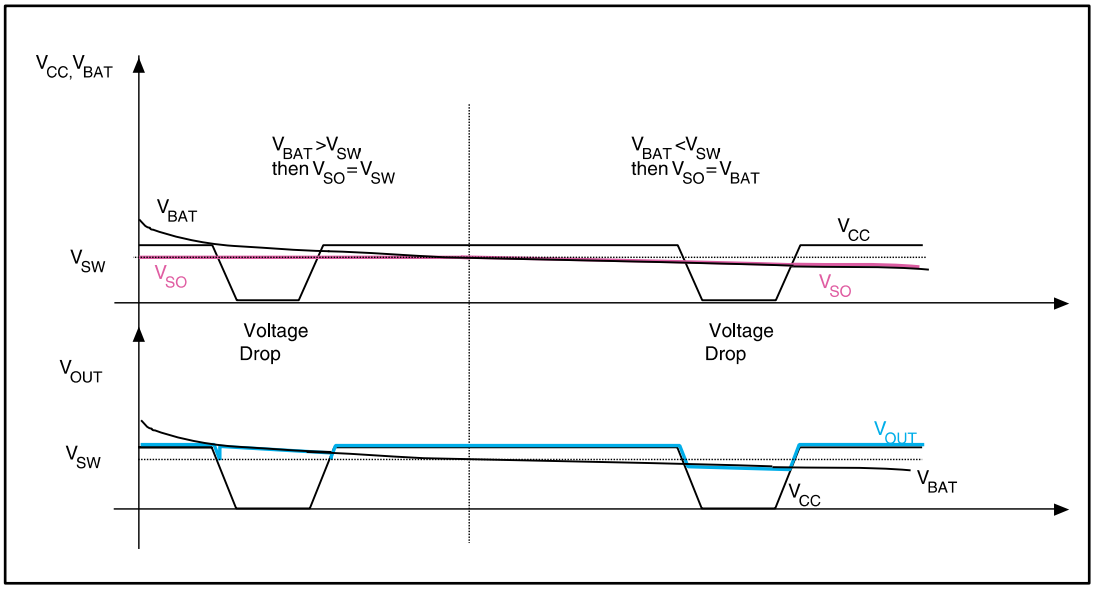


5.1 Switchover waveforms for the STM806R supervisor

The battery backup switchover voltage (V_{SO}) depends on the battery voltage (V_{BAT}) and on the switchover threshold, V_{SW} (see *Figure 11: "Battery switchover waveforms for the STM806R supervisor"*). If V_{SW} is lower than V_{BAT}, V_{SO} is equal to V_{SW}. If V_{SW} is greater than V_{BAT}, V_{SO} is equal to V_{BAT}.

Whenever V_{CC} falls below V_{SO}, the V_{OUT} output is connected to the battery, V_{BAT} (see *Figure 11: "Battery switchover waveforms for the STM806R supervisor"*).

Figure 11: Battery switchover waveforms for the STM806R supervisor



Note: The red line represents the switchover voltage (V_{SO}). The blue line represents the battery switchover circuit output voltage (V_{OUT}), which is switched to V_{CC}, or to V_{BAT} depending on the voltage magnitude.

STM806R has a voltage hysteresis of 40 mV, which gives it good noise immunity. The hysteresis depends on V_{BAT} and V_{SW} as illustrated in *Figure 12: "Switchover waveforms with hysteresis details"*:

- If $V_{BAT} > V_{SW}$ and V_{CC} falls, the battery switchover detects the switchover threshold V_{SW} and switches V_{OUT} to the backup battery supply. When V_{CC} rises, the voltage level V_{SW} + 40 mV is detected and V_{OUT} is switched back to the main power supply (V_{CC}).
- If $V_{BAT} < V_{SW}$ and V_{CC} falls, the battery switchover detects the voltage level V_{BAT} - 75 mV and switches V_{OUT} to the backup battery supply. When V_{CC} rises, the voltage level V_{BAT} - 35 mV is detected and V_{OUT} is switched back to the main power supply (V_{CC}).

Figure 12: Switchover waveforms with hysteresis details

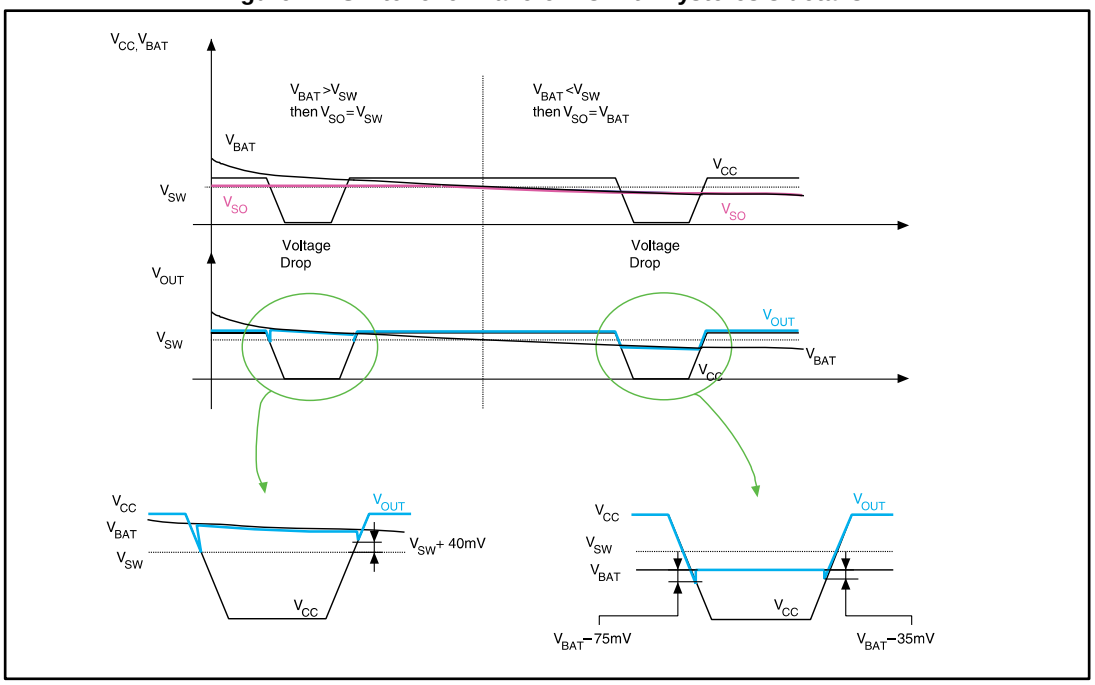


Table 8: Switchover values for the STM806R supervisor

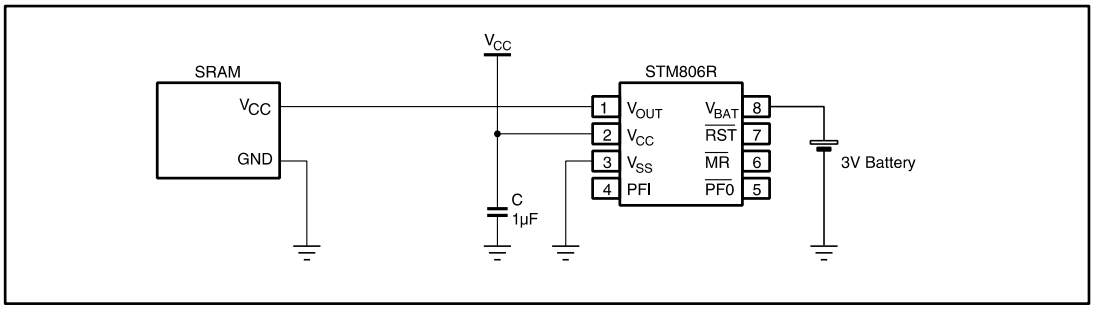
Symbol	Description	Condition	Typical Value	Unit
V_{SW}	Threshold		2.4	V
V_{hys}	Hysteresis		40	mV
V_{SO}	Battery backup switchover voltage	$V_{BAT} < V_{SW}$	$V_{SO} = V_{BAT}$	V
		$V_{BAT} > V_{SW}$	$V_{SO} = V_{SW}$	V

5.2 Hardware hookup for the STM806R supervisor

Figure 13: "Hardware hookup for the STM806R supervisor" shows one particular hardware hookup, using the STM806R Supervisor to switch the power supply source, with good efficiency and without introducing any switching noise.

In this case, the battery switchover backups the main power supply of MCU, memories and other peripherals. If sufficient power is available from the backup supply, the system can continue working normally. However it is also possible to run a safeguard routine, and to force the system to the low-power mode, so that the backup power supply can last longer, until the main power supply is restored.

Figure 13: Hardware hookup for the STM806R supervisor

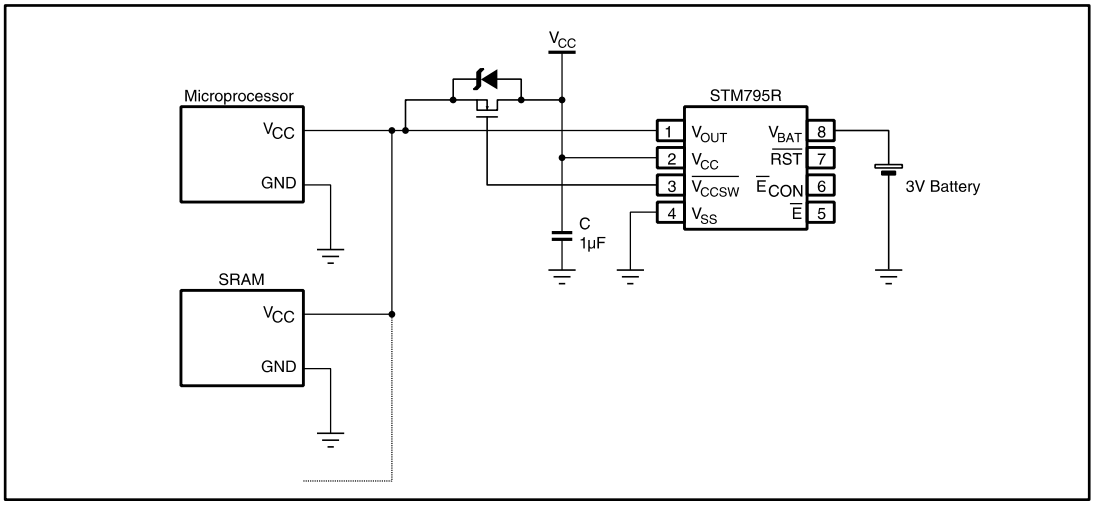


5.3 Hardware hookup for the STM795 supervisor

The V_{OUT} output is able to switch 75 mA (maximum). If the peripherals have greater current needs, it is possible to use the $\overline{Vccsw}$ output of the STM795 device, and to drive the gate of the external PMOS transistor (as shown *Figure 14: "Hardware hookup for the STM795 supervisor"*).

When V_{OUT} switches to the battery, $\overline{Vccsw}$ goes high. When V_{OUT} switches back to V_{CC}, $\overline{Vccsw}$ goes low again, and the transistor provides current directly from the power supply.

Figure 14: Hardware hookup for the STM795 supervisor



6 Chip-enable gating

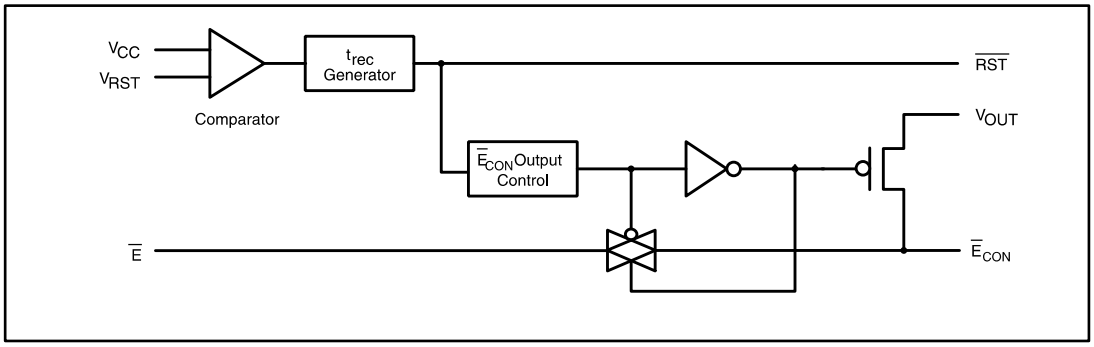
Internal gating of the chip enable signal prevents erroneous data from corrupting the external SRAM, in the event of an undervoltage condition. The chip enable signal, which normally goes directly from the microcontroller to the SRAM, is routed instead through the supervisor device. The short propagation delay enables the chip-enable gating to be used with most microcontrollers.

During normal operation (when reset is not asserted), the chip-enable signal is transmitted through the supervisor device unaltered. When reset is asserted, the SRAM is placed in its low-power mode and the memory is inaccessible. In this way, the SRAM contents are protected from data corruption.

Chip-enable gating uses a series transmission gate from $\overline{E}$ to $\overline{E}_{CON}$ (see *Figure 15: "Chip-enable gating block diagram"*). During normal operation (with reset not asserted), the $\overline{E}$ transmission gate is enabled, and passes all $\overline{E}$ transitions. At that time, the impedance of $\overline{E}$ appears as a resistor, typically about 40 Ω, in series with the load at $\overline{E}_{CON}$.

When reset is asserted, the transmission path becomes disabled. In the disabled mode, $\overline{E}$ becomes high impedance, the transmission gate is turned off, and an active pull-up connects $\overline{E}_{CON}$ to V_{OUT}. This pull-up turns off again, when the transmission gate is enabled.

Figure 15: Chip-enable gating block diagram



Note: Connect $\overline{E}$ to V_{SS} if unused.

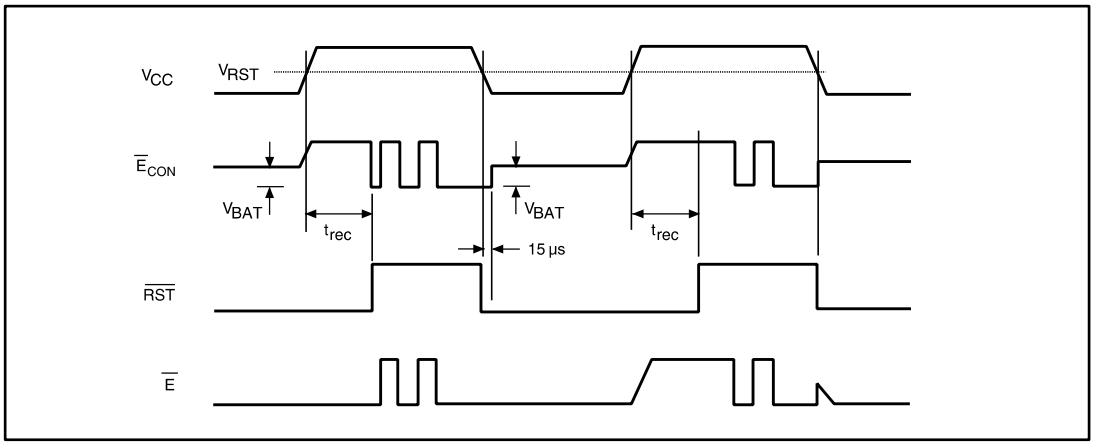
6.1 Typical waveforms for the STM818 supervisor

After power-up, the $\overline{E}_{CON}$ output stays high for a period of t_{rec} (see *Figure 16: "Typical waveforms for the STM818 supervisor"*). After this it starts to pass the $\overline{E}$ input signal on.

While reset is asserted, the chip-enable transmission gate is disabled, $\overline{E}$ is high impedance, and an active pull-up connects $\overline{E}_{CON}$ to V_{OUT} (disabled mode). If the voltage at $\overline{E}$ is high during a power-down sequence (when V_{CC} passes the reset threshold), the chip-enable transmission gate is disabled, and $\overline{E}$ immediately becomes high impedance. If $\overline{E}$ is low when reset is asserted, the chip-enable transmission gate will be disabled 15 µs after reset is asserted. This permits the current write cycle to complete during power-down.

Any time a reset is generated, the chip-enable transmission gate remains disabled, and $\overline{E}$ remains high impedance (regardless of any activity on $\overline{E}$) for the reset time-out period. The propagation delay through the chip-enable transmission gate depends on V_{CC}, the source impedance of the drive connected to $\overline{E}$, and the loading on $\overline{E}_{CON}$. For the minimum propagation delay, minimize the capacitive load on $\overline{E}_{CON}$ and use a low-output impedance driver.

Figure 16: Typical waveforms for the STM818 supervisor



Note: The chip enable gating function is also implemented on the STM795 device. Nevertheless there are two differences, in comparison to the STM818. Firstly the $\overline{E}_{CON}$ signal is held high only for half of the t_{REC} period, and secondly the chip-enable transmission gate is disabled only 10 µs after reset is asserted if the $\overline{E}$ input is low.

Table 9: Typical values for the STM818 supervisor

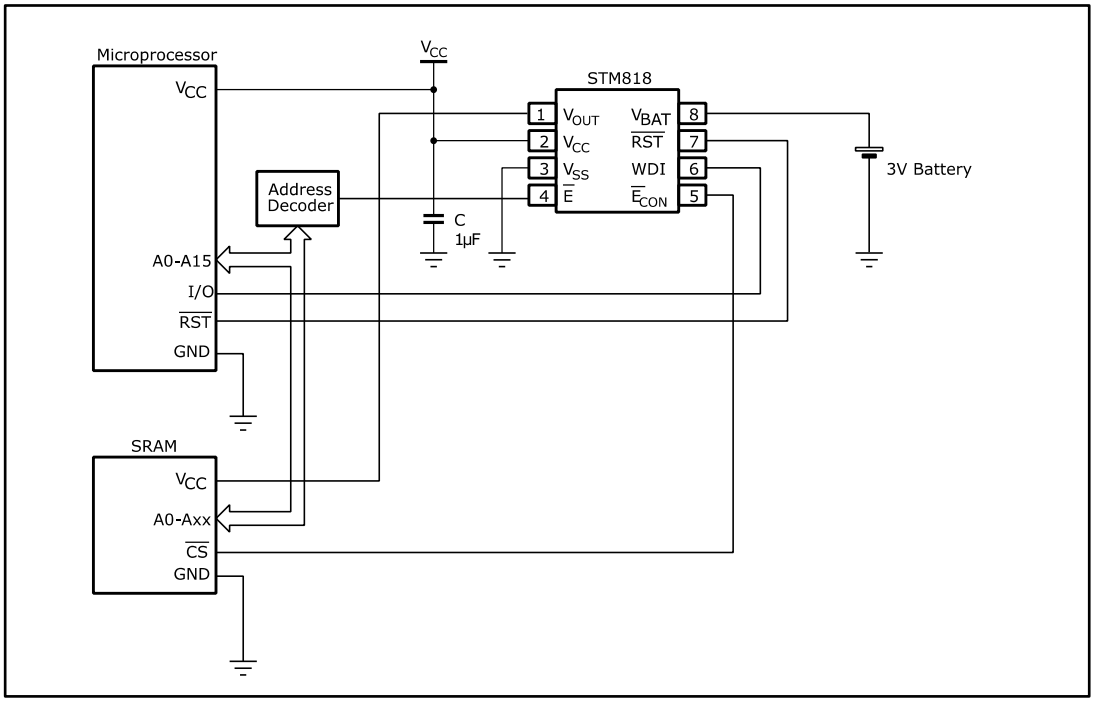
Description	Typical value	Unit
$\overline{E}$-to-$\overline{E}_{CON}$ resistance	40	Ω
Reset-to-$\overline{E}_{CON}$ high delay (power-down)	15	µs
$\overline{E}$-to-$\overline{E}_{CON}$ propagation delay	2	ns
$\overline{E}_{CON}$ short-circuit current	0.75	mA

6.2 Hardware hookup for the STM818 supervisor

Figure 17: "Hardware hookup for the STM818 supervisor" illustrates the hookup of the STM818 supervisor circuit connected to a microprocessor and an SRAM memory. All the functions of the STM818 are used (battery switchover, watchdog, chip enable gating, power-on reset, low voltage detect).

The chip enable signal is decoded by the address decoder and it goes to the $\overline{E}$ input of the supervisor circuit. The $\overline{E}_{CON}$ output is connected to the $\overline{CS}$ (chip select input) of the SRAM memory.

Figure 17: Hardware hookup for the STM818 supervisor



7 Battery freshness seal

The battery freshness seal is a feature that is available on the STM817/818/819. It disconnects the backup battery from the internal circuitry and V_{OUT} until it is needed. This allows an OEM (Original Equipment Manufacturer) to ensure that the backup battery connected to V_{BAT} will still be fresh when the final product is put to use.

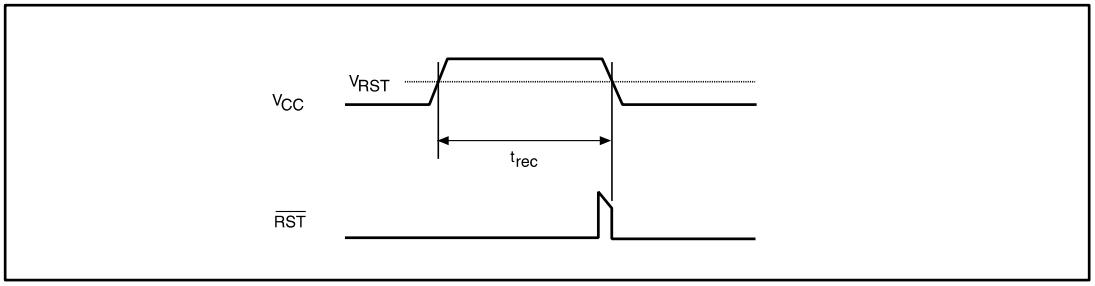
To enable the freshness seal on the STM817 and STM819:

1. Connect a battery to V_{BAT}
2. Ground $\overline{PFO}$
3. Bring V_{CC} above the reset threshold voltage, and hold it there until reset is deasserted, following the reset timeout period
4. Bring V_{CC} low again (see *Figure 18: "Typical waveforms for the STM817/818/819 supervisors"*).

For the STM818, use the same procedure, but ground $\overline{E}_{CON}$ instead of $\overline{PFO}$.

Once the battery freshness seal has enabled (disconnecting the backup battery from internal circuitry and anything that is connected to V_{OUT}), it remains enabled until V_{CC} is next brought above V_{RST}.

Figure 18: Typical waveforms for the STM817/818/819 supervisors



Note:

1. For the STM818, $\overline{E}_{CON}$ is held low, externally. The $\overline{E}_{CON}$ state is latched half way through the t_{REC} period, and the freshness seal function is enabled.

2. For the STM817 and STM819, $\overline{PFO}$ is held low, externally. The $\overline{PFO}$ state is latched half way through the t_{REC} period, and the freshness seal function is enabled.

8 Conclusion

ST's microprocessor supervisors have a large range of features adapted to the user's needs:

- Centralised function for managing a system reset
- Early warning of power failure, in time to initiate any safeguard routines
- Watchdog timer, monitoring for cessation of normal processor activity
- Battery switchover, either to allow continued operation, or to maintain minimum functionality. Also useful for the regulation of noisy power supplies
- Battery freshness seal, for maintaining the battery life on the production line, for the end user

ST's microprocessor supervisors are the ideal choice for adding protection to applications that are used in noisy environments and require power supply monitoring for proper operation.

9 References

- AN1772: How to control power-up/reset and monitor the voltage in microprocessor systems using ST reset circuits.
- AN1336: Power-fail comparator for NVRAM supervisory devices.

10 Revision history

Table 10: Document revision history

Date	Version	Revision Details
15-Mar-2005	1	First issue
27-Aug-2015	2	Removed TIMEKEEPER supervisors from *"Introduction"* Removed package specification from figures

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