AN1948
Application note

DVD combo power supply with the VIPer53-E

Introduction

The VCR is available on the market despite of the presence of the DVD readers. This document offers a typical solution to efficient supply applications where logic, DC motor drive and LCD display are implemented together in the 35 W power range and with any input voltage standard (85 Vac to 265 Vac).

Low standby consumption and cost saving meet the market needs and the key features for this application are shown in *Table 1*:

Figure 1. VIPer53-E board

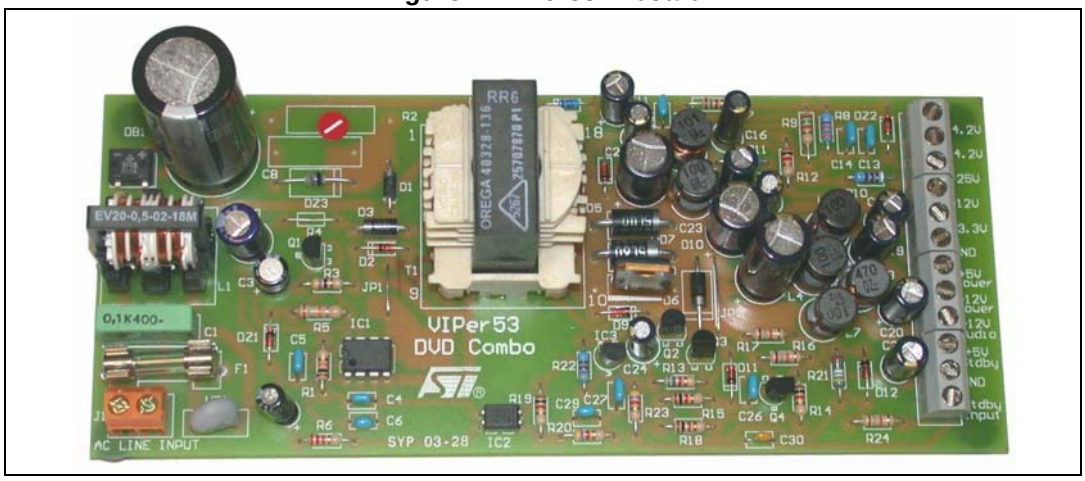


Table 1. Output specifications

	Voltage +/-5%	Maximum current	Output power	Maximum power	Board size L x W x H
Output 1	3.3 V	1.5 A	4.95 W	Normal operation: 35 W max. output power Standby operation: 750 mW max. input power with 40 mA on the 5 V standby output	170 x 70 x 40 (mm)
Output 2	5 V standby	100 mA	500 mW		
Output 3	5 V power	1.5 A	7.5 W		
Output 4	12 V power	1.5 A	18 W		
Output 5	12 V audio	200 mA	2.4 W		
Output 6	-12 V power	15 mA	180 mW		
Output 7	-25 V	25 mA	625 mA		
Output 8	4.2 V display	50 mA	210 mA		

Contents

1 Description

The VIPer53-E is the first multichip device of the VIPer® family with a very low $R_{(DS)on}$ = 1 Ω, which can go up to 35 Ω in a standard DIP8 package without the heatsink. It meets the high efficiency and reduced space features thanks to a lower power dissipation.

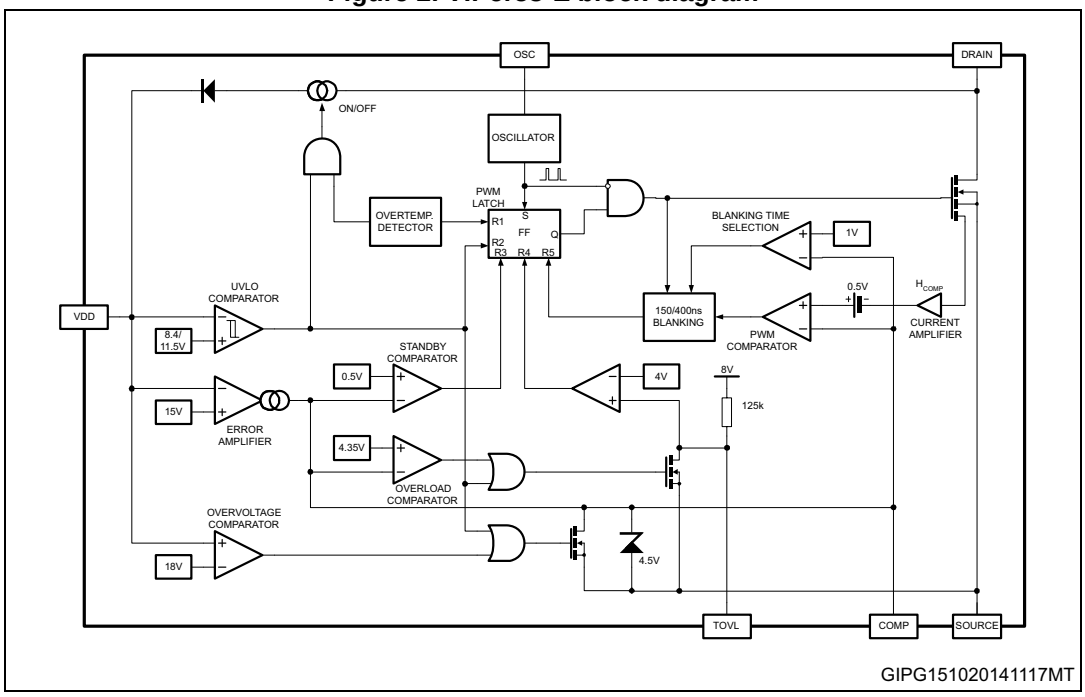
1.1 General features

The block diagram can be seen in *Figure 2*. An adjustable oscillator drives a current controlled PWM to a fixed switching frequency. The peak drain current is set for each cycle by the voltage present on the COMP pin. The useful range of the COMP pin extends from 0.5 V to 4.5 V, with a corresponding drain current range from 0 A to 2 A.

This COMP pin can be used either as an input, in case of secondary feedback configuration, or as an output when the internal error amplifier connected on the VDD pin operates in primary feedback to regulate the VDD voltage to 15 V.

The VDD undervoltage comparator drives a high voltage start-up current source, which switches off during the normal operation of the device. This feature, together with the burst mode capability, allows a very low level of input power to be reached in standby mode, when the converter is lightly loaded.

Figure 2. VIPer53-E block diagram



1.2 Overload protection

A 4.35 V typical threshold is present on the COMP pin. This overload threshold is 150 mV below the clamping voltage of 4.5 V which corresponds to the current limitation of the device. In case of a COMP voltage exceeding the overload threshold, the pull-up resistor on the TOVL pin is released and the external capacitor connected on this pin begins to charge. When a value of 4 V typical is reached, the device stops switching and remains in this state until the V_{DD} voltage reaches V_{DDoff}, or resumes normal operation if the COMP voltage returns to a value below the overload threshold. The drain current that the device delivers without triggering the overload threshold is called “current capability”, specified as I_{Dmax} in the datasheet. This value must be used to correctly size the converter versus its maximum output power. When an overload occurs on secondary side of the converter, the output power is limited by the current limitation of the device. If this overload lasts for more than a time constant defined by a capacitor connected on the TOVL pin, the device is reset, and a new sequence restarts by turning on the start-up current source. The capacitors on the VDD pin and on the TOVL pin are defined together in order to insure a correct startup and a low restart duty cycle in overload or short-circuit operation. Here are the typical corresponding formulas:

$$C_{OVL} > 12.5 \cdot 10^{-6} \cdot tss$$

$$C_{VDD} > 8 \cdot 10^{-4} \cdot \left(\frac{1}{D_{RST}} - 1 \right) \cdot \frac{C_{OVL} \cdot I_{DDch2}}{V_{DDhyst}}$$

$$C_{VDD} > \frac{I_{DD1} \cdot tss}{V_{DDhyst}}$$

Where tss and D_{RST} are respectively the time needed for the output voltages to pass from 0 V to their nominal values at startup, and the restart duty cycle in overload or short-circuit condition. A typical value of 10% is generally set for this last parameter, as it insures that the output diodes and the transformer don’t overheat. The other parameters can be found in the datasheet of the device. As the V_{DD} capacitor has to respect two conditions, the maximum value is retained to define its value.

1.3 Standby operation

On the opposite load configuration, the converter is lightly loaded and the COMP voltage decreases until it reaches the shutdown threshold typically 0.5 V. At this point, the switching is disabled and energy doesn’t pass on the secondary side. So, the output voltage decreases and the regulation loop rises again above the shutdown threshold, thus resuming the normal switching operation. A burst mode with pulse skipping takes place, as long as the output power is below the one corresponding to the minimum turn-on of the device. As the COMP voltage works around 0.5 V, the peak drain current is very low (it is defined by the

minimum turn-on time of the device, and by the primary inductance of the transformer) and no audible noise is generated.

In addition, the minimum turn-on time depends on the COMP voltage. Below 1 V (V_{COMPbl}), the blanking time increases till 400 ns, whereas it is 150 ns for higher voltages. The minimum turn-on times resulting from these values are respectively 600 ns and 350 ns, when the internal propagation time is taken into account. This feature gives the following benefits:

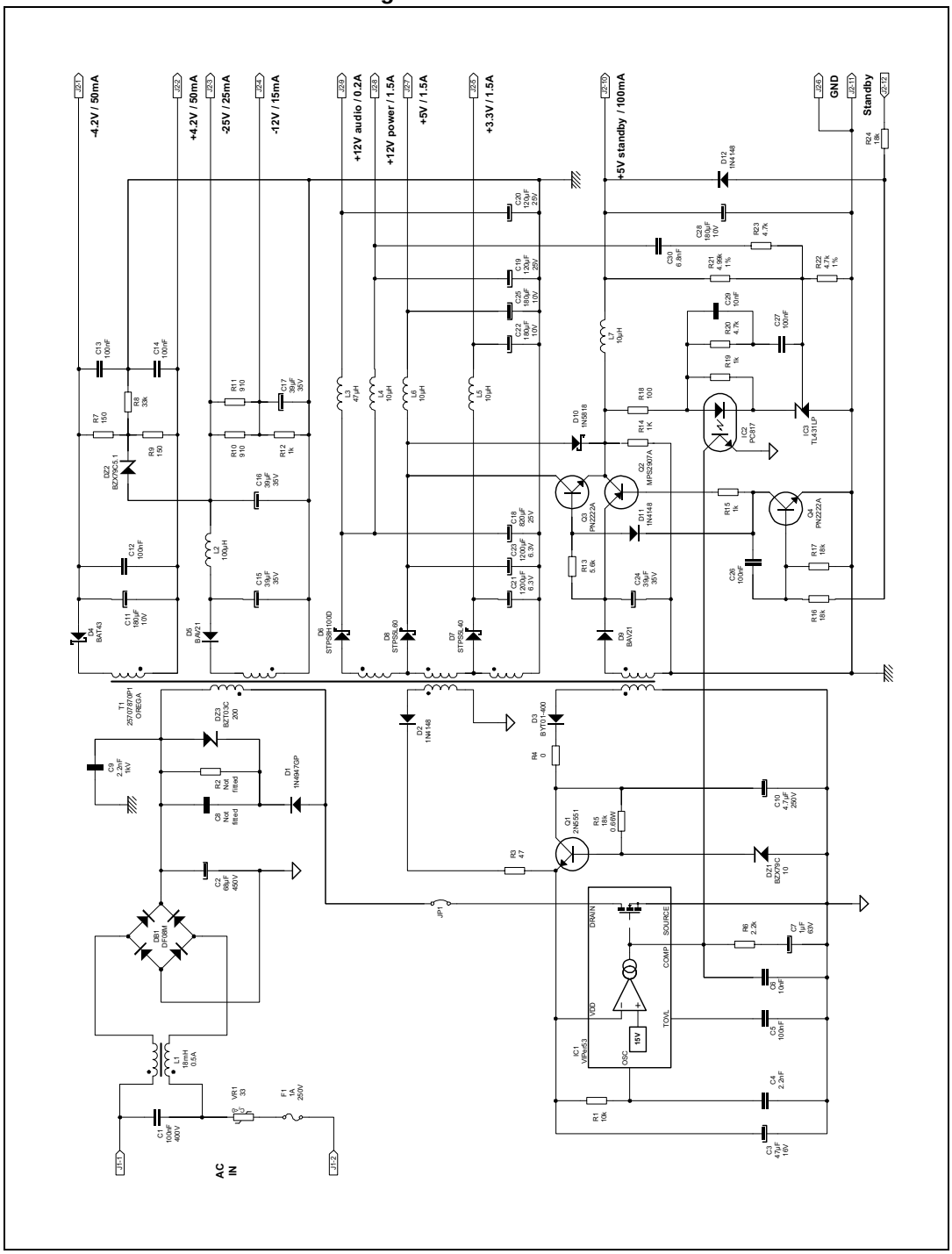
- this brutal change induces the hysteresis between normal operation and burst mode, which is reached earlier when the output power decreases.
- a short value in normal operation insures a good drain current control in case of short-circuit on the secondary side.
- long value in standby operation reinforces the burst mode by skipping more switching cycles, thus decreasing switching losses.

More details regarding the standby operation can be found in the datasheet.

2 DVD combo power supply

2.1 Schematics

Figure 3. Schematics



2.1.1 Normal operation mode

In this mode, the standby input is driven low, Q4 and Q2 are blocked and Q3 conducts. All output voltages are delivered to the loads and both 5 V and 5 V standby outputs are provided.

The transformer turn ratio leads to a voltage of about 30 V across C24. This voltage is blocked by Q2, and the 5 V standby output derives from the main 5 V output through Q3. In the case where no load is connected on the 5 V standby output, R14 allows the Q3 base current delivered by R13, to be absorbed.

The same applies to the primary side for the auxiliary supply of IC1. In normal operation, the VDD pin energy is delivered by the standard auxiliary winding through D2. The corresponding voltage is higher than the one developed by the Zener diode DZ1 on the base of Q1, and this transistor is blocked. In the meantime, the second auxiliary winding delivers five times more voltage than the one needed in standby mode (see *Section 2.1.2*), and as high values as 130 V can be observed across C10. As a consequence, C10, D3 and Q1 are high voltage type, and R5 may dissipate up to 1 W.

2.1.2 Standby mode

All output voltages drop down, except the 5 V standby one which supplies an infrared receiver and its decoding circuit, makes Q4 and Q2 conducting, and disables Q3 thanks to D11.

As Q2 conducts, the 5 V standby output is supplied through D9 and the corresponding winding of the main transformer. This winding therefore reduces its voltage by a ratio of about 5, because the regulation loop still maintains the value of 5 V on this output. Since all outputs are coupled together on the same transformer core, they are all divided by a ratio of about 5. This is sufficient to insure a reduced consumption mode, as the loads are now supplied with a much lower voltage.

D11 is needed in this mode to turn off Q3 efficiently. Otherwise, its base remains high as it is supplied by R13 connected to a voltage of about 5 V, and some reverse current flows from the 5 V standby output to the main 5 V one.

On the primary side, the standard auxiliary winding doesn't provide a sufficient voltage, and Q1 acts as a serial regulator, with the voltage delivered by the second auxiliary winding, maintaining the VDD pin of IC1 at higher level than the disabling threshold V_{DDoff} R14 on the 5 V standby output. It provides a minimum consumption in this mode to insure a suitable voltage for Q1.

The transition between the normal mode and the standby mode is slowed down by C26. This avoids any under or overvoltage on the outputs during this event. See also the following section.

2.1.3 Regulation

The regulation sets the DC operating point from the 5 V standby output through R21 and R22. Note that it is difficult to implement a split regulation, as the other outputs operate with a different value when in standby mode. Some AC signals are also introduced into the regulation loop to insure stability. The conventional path is given by R18 connected to the 5 V standby output, but another AC component has been added thanks to C30 and R23 connected on the 12 V power output. This avoids instability in situations where the 5 V standby output is lightly loaded versus the 12 V one. In order to transmit this

signal, a resistance R20 is also added in series with the conventional capacitive feedback C27 at the level of IC3.

The bandwidth of this regulation loop is set a few kHz in order to insure a good dynamic response when submitted to load variations, or during the transitions between the normal mode and the standby mode.

C29 on secondary side and C6 on primary side cancel any switching noise which may produce subharmonic operation.

2.1.4 Drain voltage clamping

The board comes with a Zener (DZ3) clamp type on the drain of the VIPer53-E device. An R-C type clamping network replaces this Zener. The corresponding components R2 and C8 are to be populated according to the bill of material. See *Table 3*.

2.1.5 Short-circuit protection

This section deals with the main outputs (5 V, 12 V and 3.3 V outputs).

When in normal mode, all these outputs are protected against a permanent short-circuit. When the short-circuit is applied to the 5 V standby, the short-circuit current flows into D10 which bypasses Q3, thus avoiding its destruction. The protection is given by the overload feature of the VIPer53-E device, which leads to hiccup mode when the COMP voltage remains high for too long time. This time is adjusted by the capacitor on the TOVL pin, and at startup it authorizes a temporary overload during the charge of the output capacitors.

In standby mode, the 5 V standby output is protected by D12 only, which forces the standby signal in the low-state, and the converter returns to the normal mode where Q2 is off. This avoids the destruction of Q2 and D9 in this condition. The other outputs are not protected against a permanent short-circuit, because the converter can still regulate correctly the 5 V standby output even if one of the others is short-circuited. This is due to the high turn ratio existing between the 5 V standby winding and the other ones, and to the low consumption on this output. Nevertheless, the user can adopt one of the following options:

– these outputs can withstand a short-circuit for a few seconds. If this time is too long, the corresponding rectifying diode may blow up, and the converter enters hiccup mode because of the short-circuit presented by the blown diode on secondary side of the transformer.
– additional diodes similar to D12 can be implemented on the other outputs to force the converter to the normal mode, where it can withstand permanent short-circuit on the main outputs.

2.1.6 Plasma display outputs

A whole set of outputs is dedicated to the driving of a plasma display: negative 25 V and 12 V outputs, together with a symmetrical +/-4.2 V centered 5 V higher than the -25 V output voltage.

These outputs are not protected against short-circuits or overloads. For instance, the short-circuit of the 4.2 V outputs to ground leads to the destruction of R7 or R9. Besides, the rectifying diodes chosen for these outputs don't withstand a permanent short-circuit.

Figure 4. Startup in normal mode

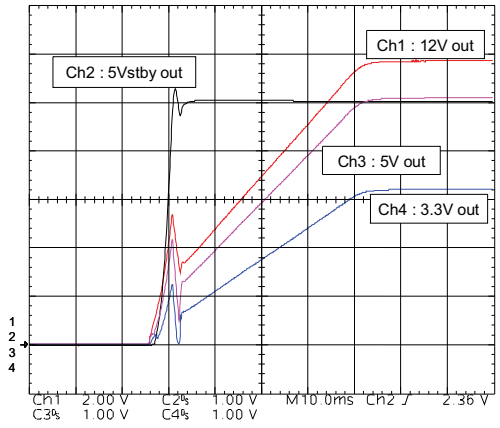
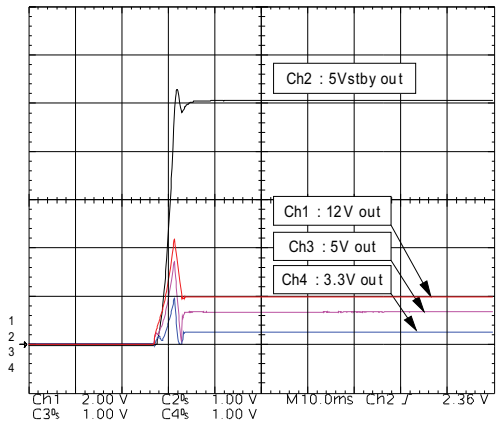


Figure 5. Startup in standby mode



2.2 Results

Unless otherwise specified, these tests are at 300 V_{dc} input voltage and full load.

2.2.1 Startup

When starting, C26 is discharged, and the converter operates in standby mode. So, the 5 V standby voltage appears first, and the other outputs rise slowly, just like a transition from a standby mode to the normal one. Of course, if the standby signal is asserted high (active level), the converter remains in this mode and the 5 V standby output is delivered only. This is illustrated in *Figure 4* and *5*.

The input voltage doesn't impact on the dynamic behavior of the converter. The rising slope of the output voltage at startup is mainly governed by the charge of C26 with the current defined by the base to emitter voltage of Q4 together with R16 and R17.

2.2.2 Switch-off

Figure 6 presents the output voltages at switch-off of the converter. All voltages drop down at the same time, because the converter doesn't deliver energy any more. So, slopes are individually driven by the output capacitors and the output current.

Figure 6. Switch-off

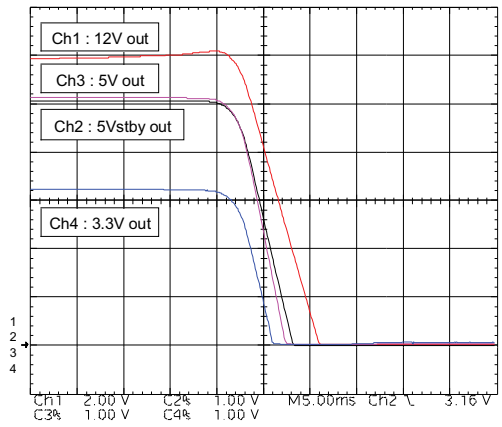


Figure 7. Normal to standby mode transition

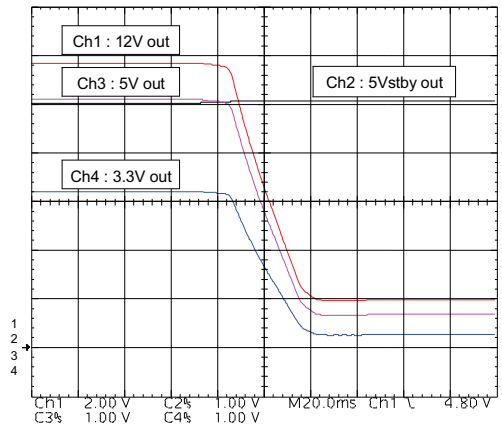


Figure 8. Standby to normal mode transition

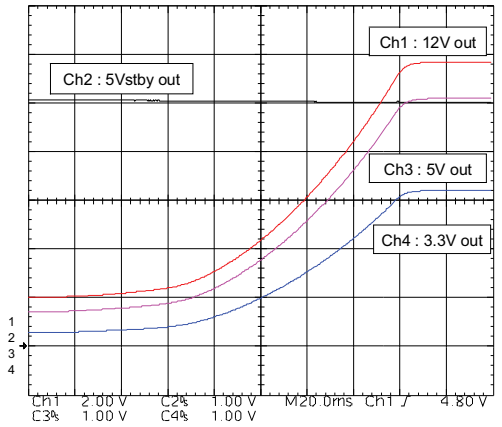
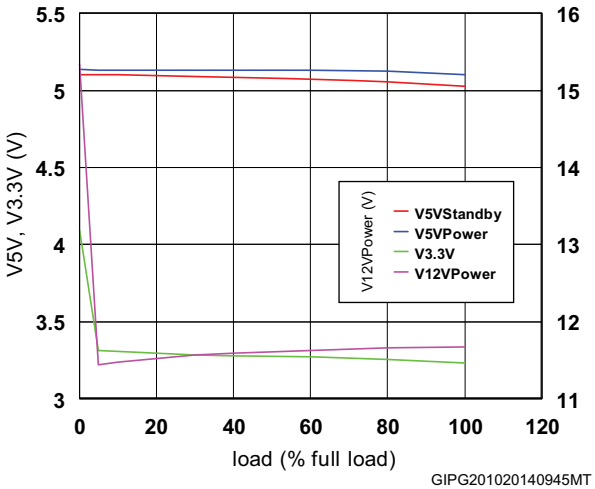


Figure 9. Load regulation



2.2.3 Transitions between normal and standby mode

The standby input is quickly driven from low-state to high-state, and inversely. The corresponding evolution of the output voltages are shown in *Figure 7* and *8*. To be noted the very low disturbance on the 5 V standby output.

2.2.4 Load and cross regulation in normal mode

For these tests, the 12 V audio output is always opened. As it is connected almost in parallel with the 12 V power output (only an L-C filter), it is assumed to follow the same voltage variation as this output, and its current is added to the power one.

Also, load variation is on the main power outputs: 5 V standby, 5 V power, 3.3 V and 12 V power. -25 V and +/-4.2 V secondary outputs are either not loaded (load regulation test) or fully loaded (cross regulation test).

The load regulation is checked by changing the loads on all outputs simultaneously. This test is also used to measure the efficiency of the converter over a large range of

output power. *Figure 9* shows the corresponding results for the four main outputs and *Figure 10* for the two secondary ones. When not loaded, the converter operates correctly, except for 12 V and 3.3 V outputs which do not have any load. So, the corresponding voltages rise up respectively to 15.3 V and 4.1 V. If this is not acceptable, the user has to foresee an adequate minimum load or a clamper.

Figure 10. Cross regulation for secondary outputs

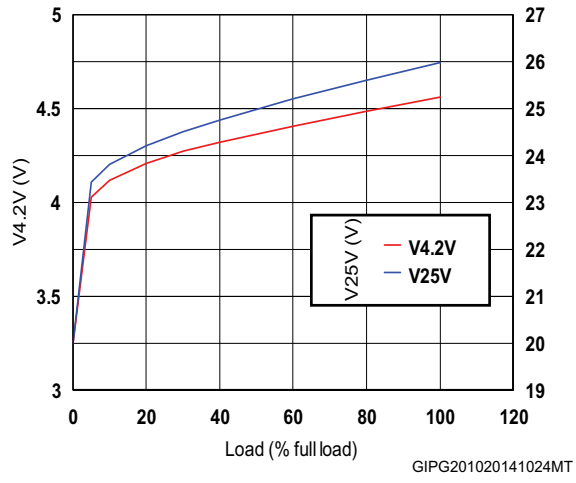
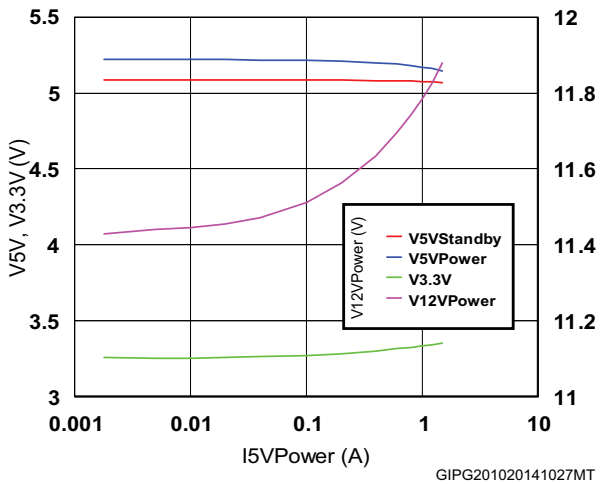


Figure 11. 5 V power cross regulation



As the load on the secondary outputs is zero during this test, *Figure 10* shows the cross regulation between the main outputs and the secondary ones. Note that the secondary output voltages don't change significantly versus their own load current, because these currents are low values, and these outputs have already been significantly loaded on the board itself. So, no load regulation is presented for the secondary outputs. The cross regulation between the main outputs has been measured. For this purpose, outputs are loaded at intermediate level (half the maximum rated load), except one output which varies between zero and maximum load. This test is repeated for the four main outputs and is presented from *Figure 11* to *14*. The result is also used to compute the relative efficiency for each main output.

Figure 12. 5 V standby cross regulation

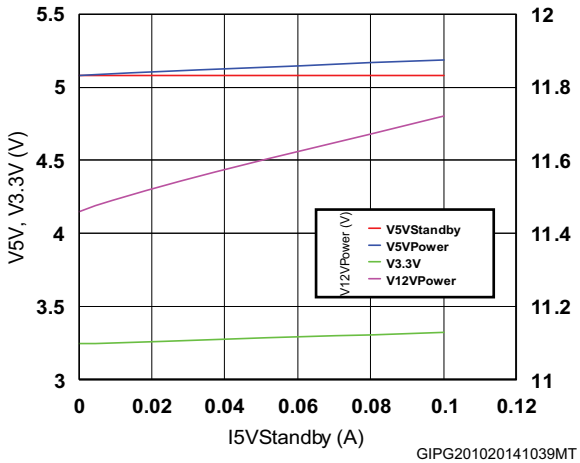


Figure 13. 3.3 V cross regulation

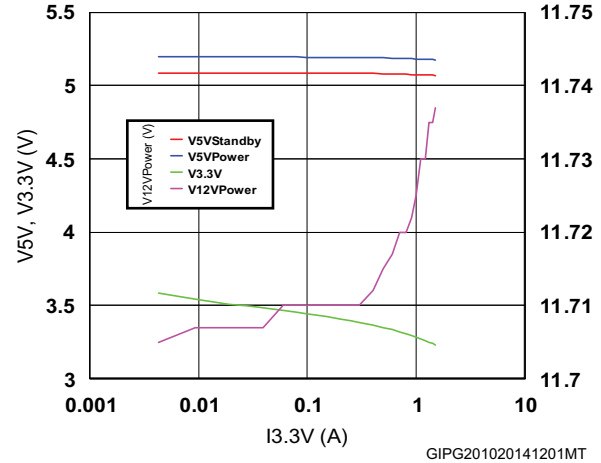


Figure 14. 12 V power cross regulation

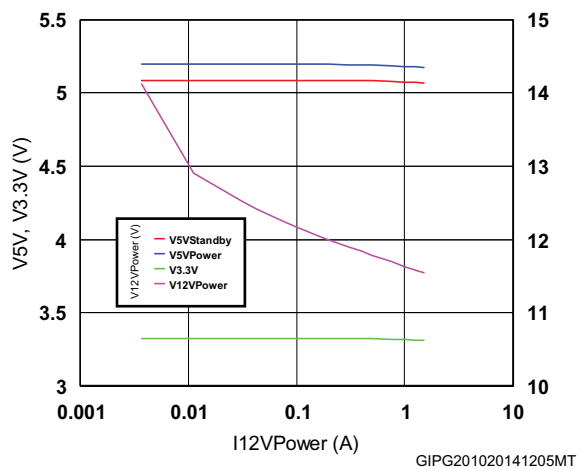
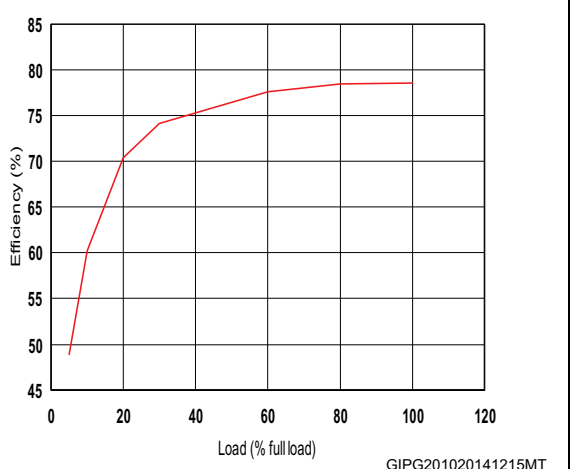


Figure 15. Global efficiency



2.2.5 Efficiency in normal mode

The global efficiency is measured by varying the output load simultaneously, except for the secondary ones (-25 V and +/-4.2 V) which are not loaded in order to get the lowest values. *Figure 15* presents the result.

Each cross regulation measurement computes the relative efficiency Er on the corresponding output by using the following formula:

Equation 1

$$E_R = \frac{P_{outmax} - P_{outmin}}{P_{inmax} - P_{inmin}}$$

The results are shown in the following table:

Table 2. Er for output

	3.3 V	5 V standby	5 V power	12 V power
Er	77%	73%	80%	85%

The lower the output voltage, the lower the relative efficiency because of the fixed voltage drop in the output rectifying diodes. The relative efficiency for the 5 V standby output is low when compared to the other ones, because of two reasons:

1) it is derived from the 5 V power output, with a voltage drop in Q2 of about 100 mV which leads to a loss of 2% in efficiency.

2) when the output current on the 5 V standby increases, its output voltage remains fixed by the regulation loop, and all the other outputs increase by 2%. So, the onboard dummy loads for the secondary outputs (R7 to R12) increase by 5% (related to the 500 mW of full load on the 5 V standby output), and the relative efficiency decreases.

Overall, the total efficiency decreases by 7%, which corresponds to the difference between the 5 V power and the 5 V standby outputs.

The efficiency has also been measured at full load and for an input voltage varying between 120 V_{dc} and 400 V_{dc}. The results are shown in *Figure 16*.

Figure 16. Efficiency vs. input voltage

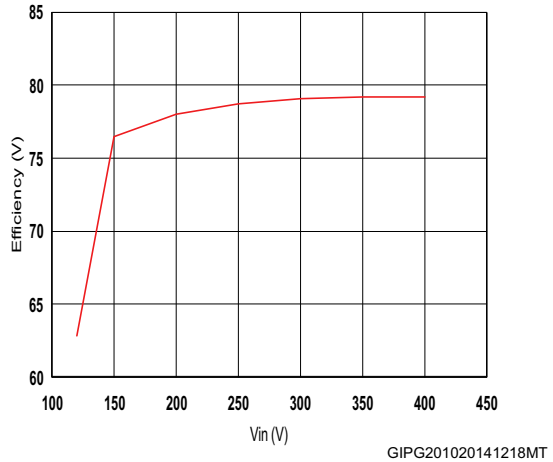
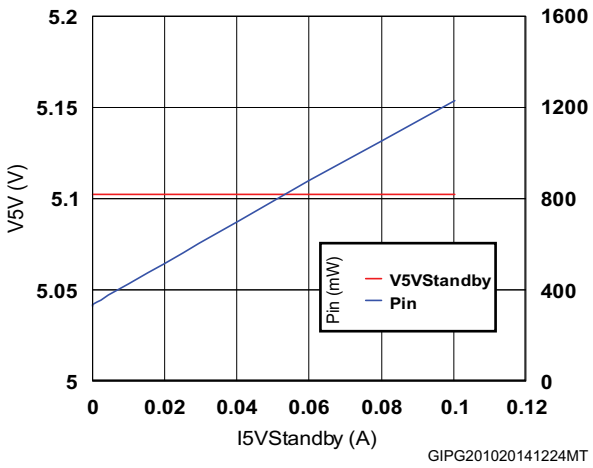


Figure 17. Load regulation and input power in standby mode



2.2.6 Load regulation and input power in standby mode

As there is only one active output in standby mode, there is no cross regulation measurement. Instead, the input power is measured to check its compliance versus specific energy saving standards like Energy Star or Blue Angel. Both output voltage value and input power are shown in *Figure 17*. All other outputs are not loaded. The user should pay attention to its real load, which may consume some power in this condition: even if the voltages are reduced by a ratio of five or more, they are still able to deliver the rated current.

At 300 V_{dc} input voltage, the converter always works in burst mode in standby condition. This mode is characterized by the fact that the device skips some switching cycles, as shown in *Figure 18*. The magnification in *Figure 19* presents a conduction time of 700 ns, which corresponds to the long blanking time of the VIPer53-E device, as the COMP voltage operates around the shutdown value (0.5 V typical), well below the blanking value threshold (1 V typical). Also note the reduced reflected value versus the normal full load switching cycle in *Figure 20*.

Figure 18. Burst mode in standby condition

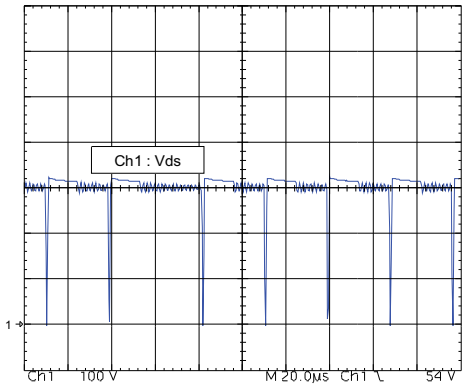


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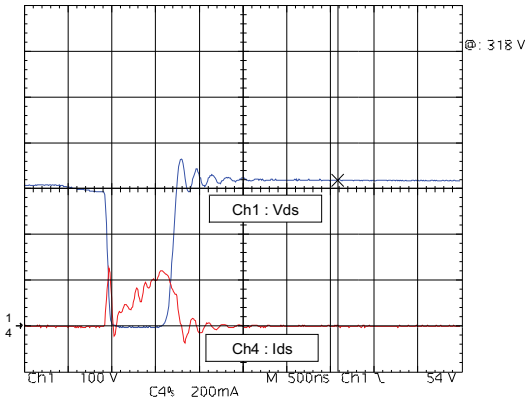
Figure 19. Magnification of a switching cycle in standby condition



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2.2.7 Line regulation

The output voltage has been measured at full load for an input voltage varying between 120 V_{dc} and 400 V_{dc} for both power (*Figure 21*) and secondary (*Figure 22*) outputs.

Figure 20. Normal full load switching cycle

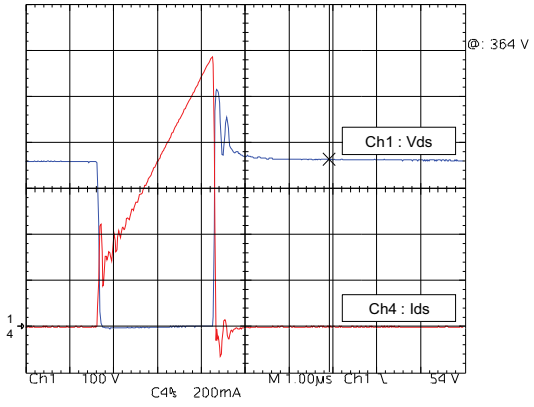

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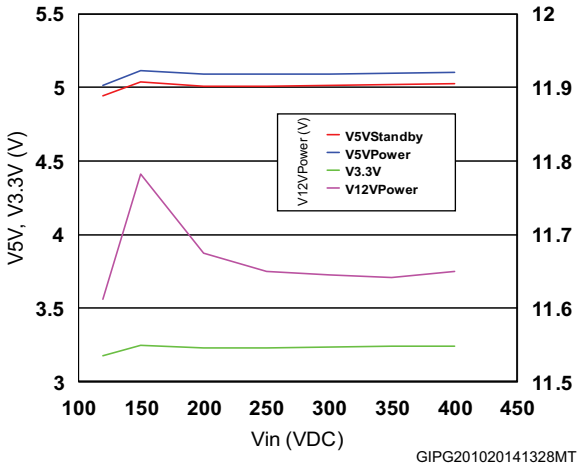
Figure 21. Line regulation for the main outputs



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2.2.8 Dynamic load variation

Each main output has been submitted to fast load variation between 10% and 100% of their rated full load. All the others are loaded with a fixed current corresponding to half load. Results are presented from *Figure 23* to *26*.

Figure 22. Line regulation for secondary outputs

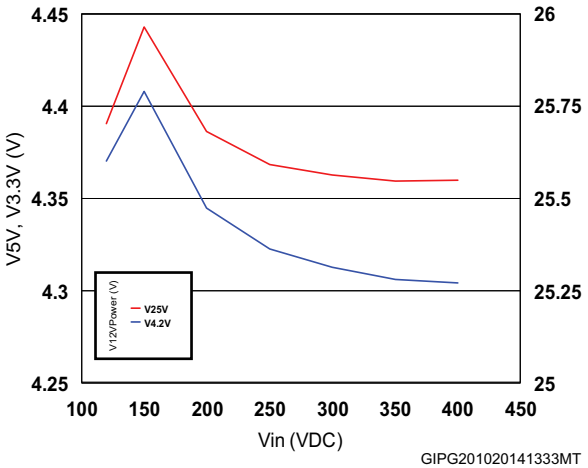

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Figure 23. 5 V power dynamic load regulation

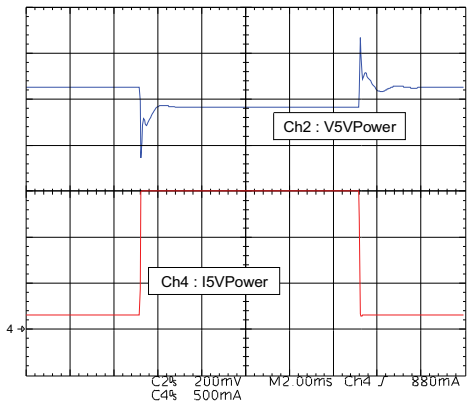

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Figure 24. 5 V standby dynamic load regulation

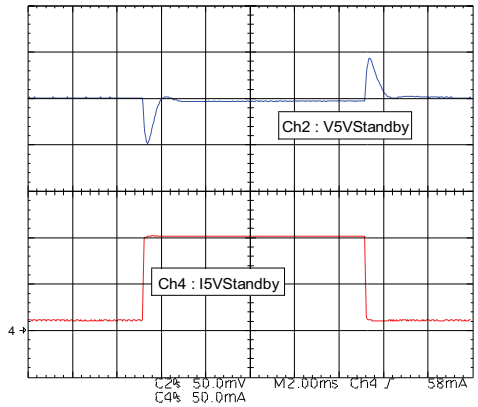

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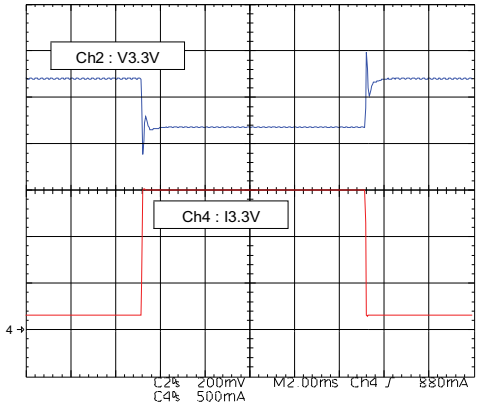
Figure 25. 3.3 V dynamic load regulation



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2.2.9 Stability

An example of stability measurement is presented in *Figure 27* at full load. The phase margin is about 50 ° with a gain margin of about 10 dB.

Figure 26. 12 V dynamic load regulation

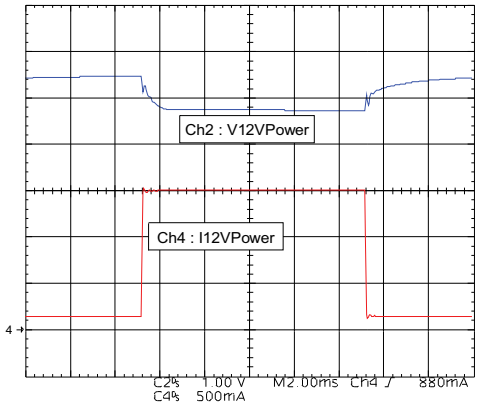

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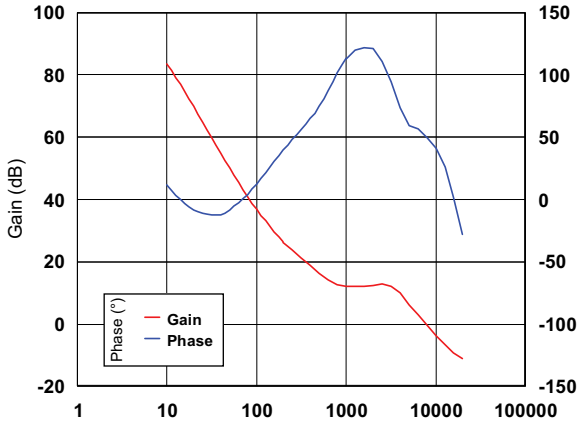
Figure 27. Gain and phase plot at full load



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2.2.10 Short-circuit operation

Refer to *Section 2.1.4* and *2.1.5* for short-circuit protections. A short-circuit is present on the 12 V power output in the normal mode. The converter protects itself by entering an endless restarting sequence, driven by the VIPer53-E V_{DD} voltage collapsing down to the V_{DDoff} threshold periodically. Note that the V_{DD} voltage doesn't decrease sufficiently during the switching operation, and that the overload feature of the device is the real protection. This is visible in *Figure 28*, where TOVL voltage rises up as soon as the COMP pin is stuck to its maximum value of about 4.5 V. When it reaches the overload threshold (about 4 V), the converter halts switching, and the V_{DD} voltage decreases a little bit and remains at 9.6 V for 30 ms. This is due to the additional auxiliary winding and associated components which discharge the energy stored in C10, and act as serial regulators. Then, the V_{DD} voltage definitely decreases until it triggers the reset voltage V_{DDoff} (8.4 V typical), and the device activates its internal high voltage start-up current source to recharge the V_{DD} capacitor C3.

The full restarting cycle can be observed in *Figure 29*. The restarting duty cycle defined as the ratio of the active phase where the VIPer53-E device switches, over the total restarting cycle, is kept about 8%. This low value prevents any overheating of the output diode and of the transformer. The short-circuit can be indefinitely applied without any stress for the converter.

Figure 28. Short-circuit protection

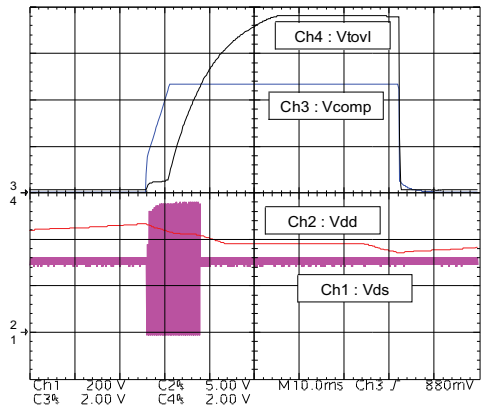

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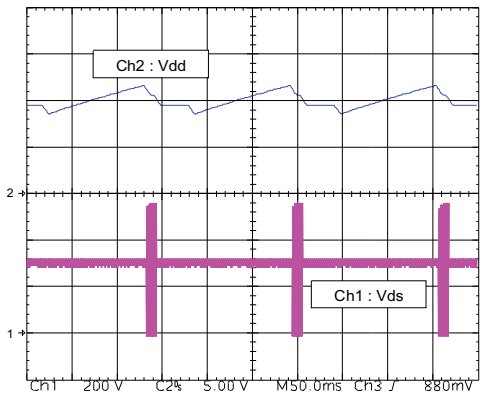
Figure 29. Restarting cycles



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2.3 Board description

Table 3. Bill of material

Quantity	Reference	Description	Note
1	D1	1N4947GP diode	
3	D2, D11, D12	1N4148 diode	
1	D3	ST BYT01-400 diode	
1	D4	ST BAT43 Schottky diode	
2	D5, D9	BAV21 Schottky diode	
1	D6	STPS8H100D Schottky diode	
1	D7	STPS5L40 Schottky diode	
1	D8	STPS5L60 Schottky diode	
1	D10	ST 1N5818 Schottky diode	
1	DZ1	BZX79C10 Zener diode	
1	DZ2	BZX79C5.1 Zener diode	
1	DZ3	BZT03C200 Zener diode	
1	DB1	DF08M diode bridge	
1	Q1	2N5551 transistor	
1	Q2	PN2907A transistor	
2	Q3, Q4	PN2222A transistor	
1	IC1	VIPer53-E SMPS controller	
1	IC2	PC817 optocoupler	
1	IC3	TL431ILP voltage reference	

Table 3. Bill of material (continued)

Quantity	Reference	Description	Note
1	C1	100 nF 20% 400 V ceramic capacitor	
1	C2	68 µF 20% 450 V electrolytic capacitor	
1	C3	47 µF 20% 16 V electrolytic capacitor	
1	C4	2.2 nF 10% 100 V ceramic capacitor	
6	C5, C12, C13, C14, C26, C27	100 nF 10% 100 V ceramic capacitor	
2	C6, C29	10 nF 10% 100 V ceramic capacitor	
1	C7	1 µF 20% 63 V electrolytic capacitor	
0	C8	6.8 nF 10% 400 V ceramic capacitor	Option - not fitted
1	C9	2.2 nF 10% 1 kV ceramic capacitor	
1	C10	4.7 µF 20% 250 V electrolytic capacitor	
4	C11, C22, C25, C28	180 µF 20% 10 V electrolytic capacitor	
4	C15, C16, C17, C24	39 µF 20% 35 V electrolytic capacitor	
1	C18	820 µF 20% 25 V electrolytic capacitor	
2	C19, C20	120 µF 20% 25 V electrolytic capacitor	
2	C21, C23	1200 µF 20% 6.3 V electrolytic capacitor	
1	C30	6.8 nF 10% 100 V ceramic capacitor	
1	R1	10K 1/4 W 5% resistor	
0	R2	22K 3 W 5% resistor	Option - not mounted
1	R3	47 1/4 W 5% resistor	
1	R4	0 resistor	
1	R5	18K 1/2 W 5% resistor	
1	R6	2.2K 1/4 W 5% resistor	
2	R7, R9	150 1/4 W 5% resistor	
1	R8	33K 1/4 W 5% resistor	
2	R10, R11	910 1/4 W 5% resistor	
4	R12, R14, R15, R19	1K 1/4 W 5% resistor	
1	R13	5.6K 1/4 W 5% resistor	
3	R16, R17, R24	18K 1/4 W 5% resistor	
1	R18	100 1/4 W 5% resistor	
2	R20, R23	4.7K 1/4 W 5% resistor	
1	R21	4.99K 1/4 W 1% resistor	
1	R22	4.7K 1/4 W 1% resistor	
1	L1	18 mH 0.5 A common mode filter	

Table 3. Bill of material (continued)

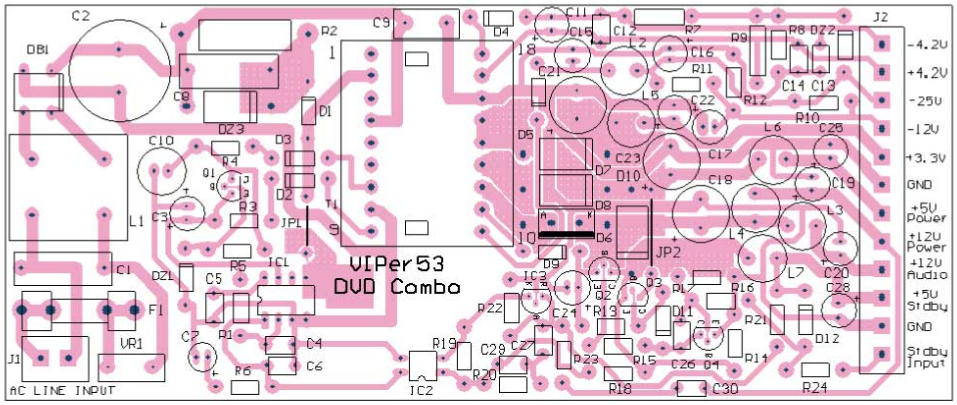
Quantity	Reference	Description	Note
1	L2	100 µH 10% 0.75 A inductor	
1	L3	47 µH 10% 1.4 A inductor	
4	L4, L5, L6, L7	10 µH 20% 4.3 A inductor	
1	T1	Thomson multimedia - Orega 25707870P1 transformer	
1	F1	250 V 1 V fuse	
2	F1	Fuse clip	
0	No reference	18 ºC/W dissipater	Option - not fitted
1	J1	2 point connector	
4	J2	3 point connector	
4	No reference	Adhesive base	1 per board angle

2.3.1 Board layout

Conventional cares have been observed when this board has been designed:

- the ground pin of IC1 (the VIPer53-E device) is a star point for two connections. The former is dedicated to the power ground line issued from C2 and the transformer T1, and the latter is reserved for all low signal components associated with this circuit. This rule should be respected in order to avoid any spurious noise to be injected on the signal pins.
- a sufficient copper area is foreseen at the level of the drain pin of IC1 and for all main secondary rectifying diodes (D6 to D8) in order to provide a heatsink capability for these devices.

Figure 30. PCB layout



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2.3.2 Transformer specifications

Table 4. Transformer specifications

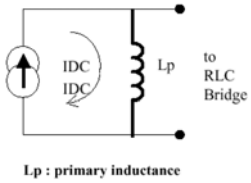
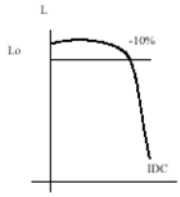
	Item	Conditions	Specifications
1	Primary inductance	Measuring points 2 and 4 Measuring frequency 1 kHz Applied voltage: 250 mV	L_p = 808 µH ± 12%
2	Leakage inductance	Measuring points: 2 and 4 Measuring frequency 10 kHz (all secondaries shorted)	See typical value
3	DC superimposed current	 Lp : primary inductance L_p: primary inductance	L = Lo x 0.9, I_{sat} = 1.8 A at 100 °C 
4	Max. primary power		45 W
5	Operating voltage		90 V - 270 V
6	Operating frequency		70 kHz fixed
7	Controller circuit		VIPer53-E
8	Regulation mode		Secondary (5 V)

Figure 31. Transformer specifications

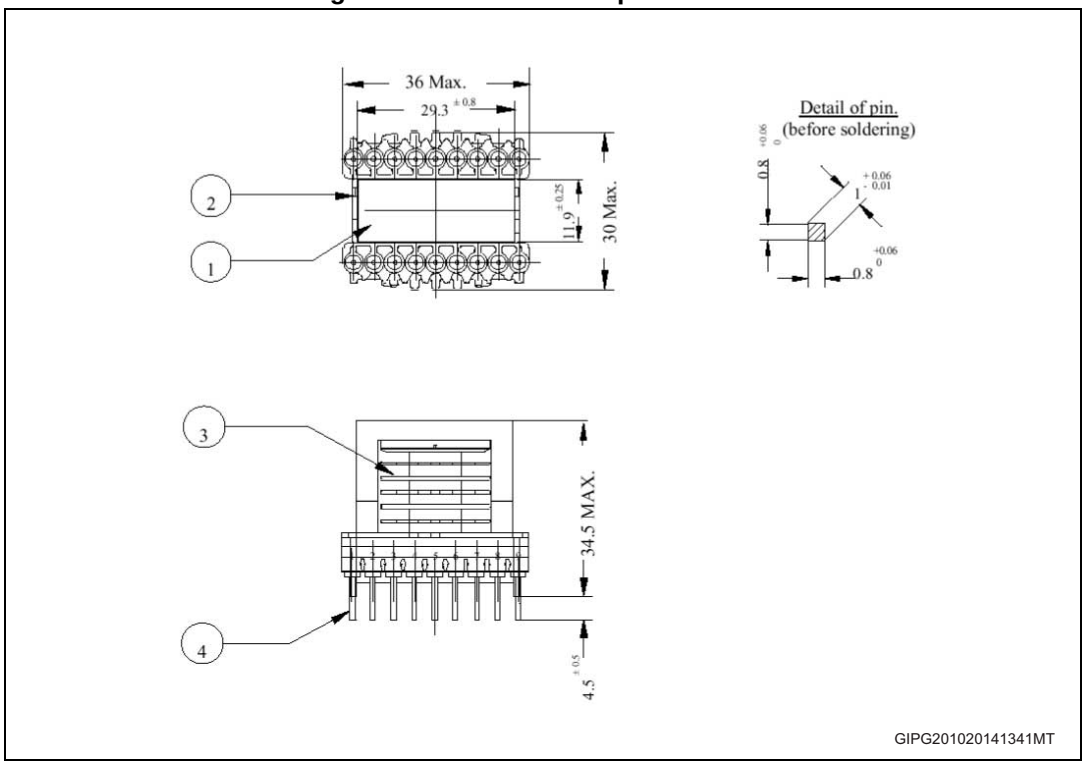


Table 5. Number of turns

Number of turns:	
Auxiliary	66 turns
Added auxiliary	66 turns
3.3 V	4 turns
5 V power	6 turns
12 V	13 turns
- 25 V	27 turns
- 4.2 V / 4.2 V	5 turns
5 V standby	28 turns

3 Revision history

Table 6. Document revision history

Date	Revision	Changes
12-Nov-2014	2	Updated title in cover page. Content reworked to improve readability, no technical changes.