AN1596
APPLICATION NOTE

VIPower: HIGH SIDE DRIVERS FOR AUTOMOTIVE

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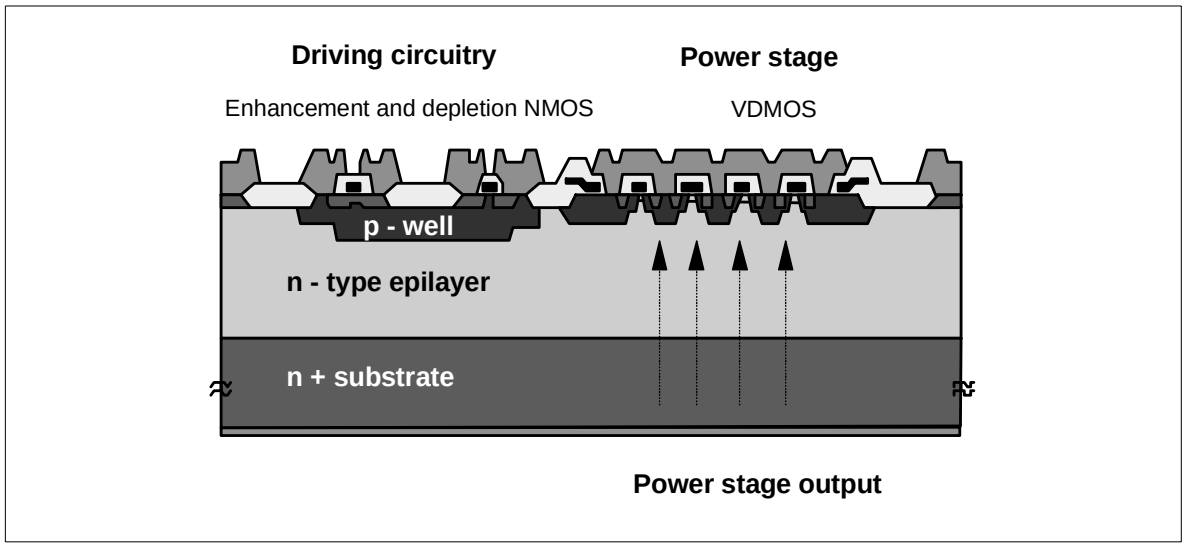
INTRODUCTION

Today's automotive market requires a continuous increasing of complexity and reliability in the electronic systems. To achieve this, the concept of the automotive systems is more and more based on micro controllers architecture driving integrated monolithic circuits that include a power stage, control, driving and protection circuits on the same chip. Vertical Intelligent Power, a STMicroelectronics patented technology, established over 13 years ago, uses a fabrication process which allows the integration of complete digital and/or analog control circuits driving a vertical power transistor on the same chip. The VIPower M0 technology used for making High Side Drivers (HSDs) produces a monolithic silicon chip, which combines control and protection circuitry with a standard power MOSFET structure where the power stage current flows vertically through the silicon (see figure 1).

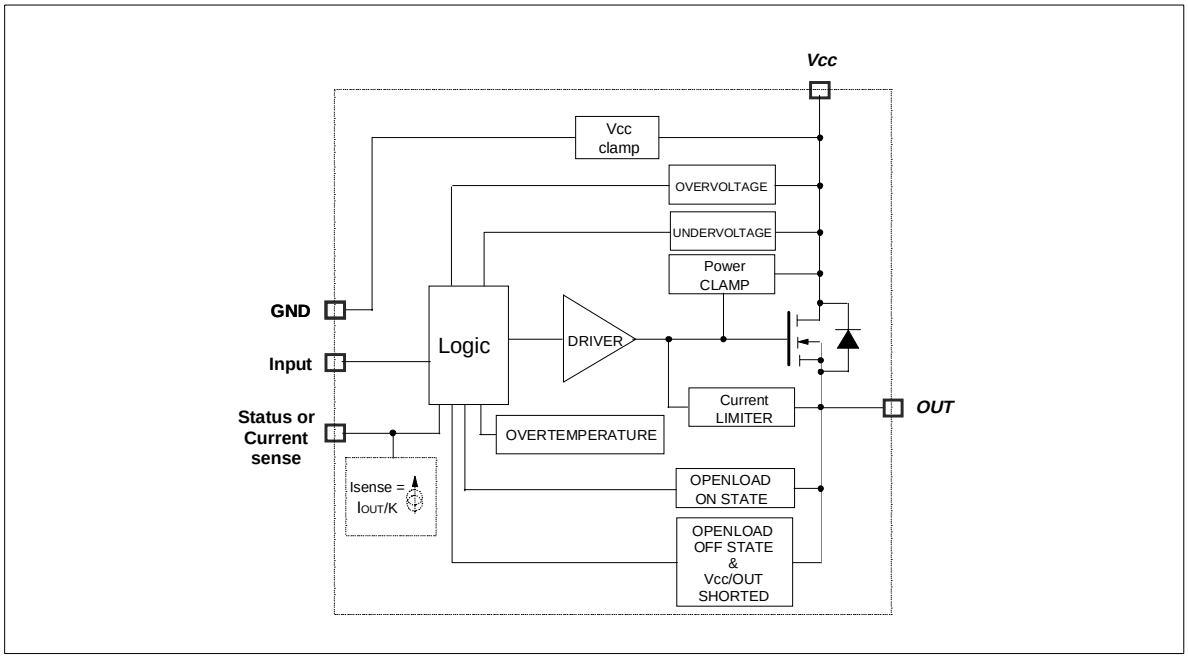
Figure 1: M0 chip structure



The evolution of M0 technology made the drastic reduction of die size and of the resistance of devices possible during conduction as well; each generation has seen a significant (from 40% to over 50%) decrease in specific on-resistance and this translates into die size reduction, smaller packages, reduced power dissipation and hence cost effective solutions. The third generation - the M0-3 - is in production while STMicroelectronics is now developing the M0-4 and M0-5 technologies which will allow to achieve less than 5mΩ $R_{DS(on)}$ in a PowerSO-10 package. High Side Drivers, with their integrated extra features are power switches that can manage high currents and work up to about 36V supply voltage. They only require a simple TTL logic input and incorporate a diagnostic output to the micro-controller. They can drive an inductive load without the need for a freewheeling diode. For complete protection the devices have an over-temperature sensing circuit that will shut the chip down under over-temperature conditions. Due to the aggressive automotive environment, High Side Drivers are designed to work from -40°C to +150°C. They also have an under-voltage shutdown feature. Each application exerts an external

influence over the switch. A filament lamp or DC motor, for example, has in-rush currents that any switch needs to handle. Solenoids and motors have an inductive effect and must lose the residual magnetism when the current is turned off. External fault conditions can also stress the drivers and their associated circuitry. The M0-3 High Side Driver can be divided in Analog and digital. This classification is done with regard to diagnostic pin, which can be a two level signal pin or an analogue current sense pin. Diagnostic information output helps the on Board microcontroller to quickly identify and isolate faults saving repair time and often improving safety. High Side Drivers can reduce the size and weight of switch modules, and where multiplexed systems are used, they dramatically reduce the size of the wiring harness.

Figure 2: Generic HSD Internal Block Diagram



STMicroelectronics HSDs are designed to provide the user with simple, self protected, remotely controlled power switches. They have the general structure as shown in figure 2.

THE GENERAL FEATURES OF HIGH SIDE DRIVERS

Input

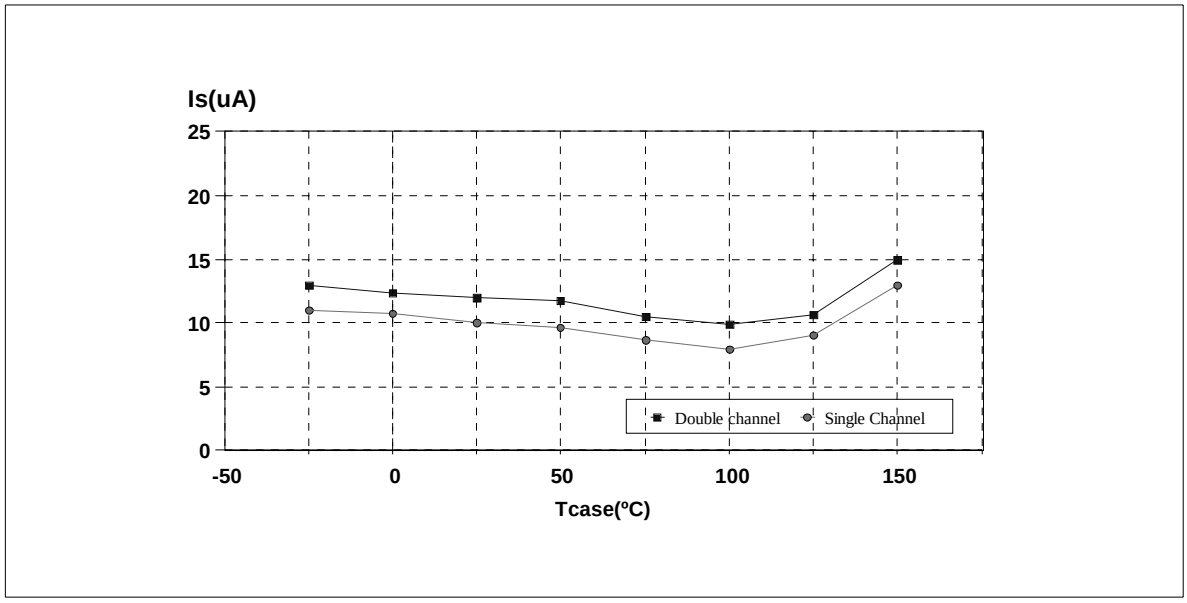
The 5V TTL input to these High Side Drivers is protected against electrostatic discharge (V_{ESD}=4kV for control pins and 5kV for Power pins). General rules concerning TTL logic should be applied to the input. The input voltage is clamped internally at V_{ICL}=6.8V as typical value. It is possible to drive the input with a higher input voltage using an external resistor calculated to give a current not exceeding I_{IN}=10mA (see datasheets absolute maximum ratings section).

Internal power Supply

To accommodate the wide supply voltage range experienced by the logic and control functions, these devices have an internal power supply. Some parts of the chip are only active when the input is high, the charge pump for example. Therefore it is possible to conserve power when the device is idle. The new M0-3 generation High Side Drivers supply current in the ON state is 5mA/channel. The internal power consumption for the basic functions of the chip under any circumstances - even when the input is 0V - is very low. The supply quiescent current I_S, guaranteed at junction temperature of 25°C, a battery voltage

of 13V and the output pin grounded, is limited to a typical value of 10µA for a one channel HSD. In figure 3 a plot of typical I_S values versus T_j is shown for single channel and double channel monolithic HSDs.

Figure 3: Stand-by current for single and double channel single chip HSDs Vs. junction temperature



Thermal considerations

In order to choose the suitable HSD for a given load some important points must be highlighted. In the worst-case operation (T_j=150ºC), for a single channel HSD and in steady state conditions, the Joule effect power developed by the device equals the Power dissipated according to the following equation:

$$R_{DS(on)} \cdot I_{OUT}^2 + V_{CC} \cdot I_S = \frac{T_J - T_{amb}}{R_{thj-amb}}$$

Assuming that the second term can be neglected, for a given load current I_{OUT} a given package and heat sink and a given ambient temperature (fixed at 85°C in automotive environment) the result is:

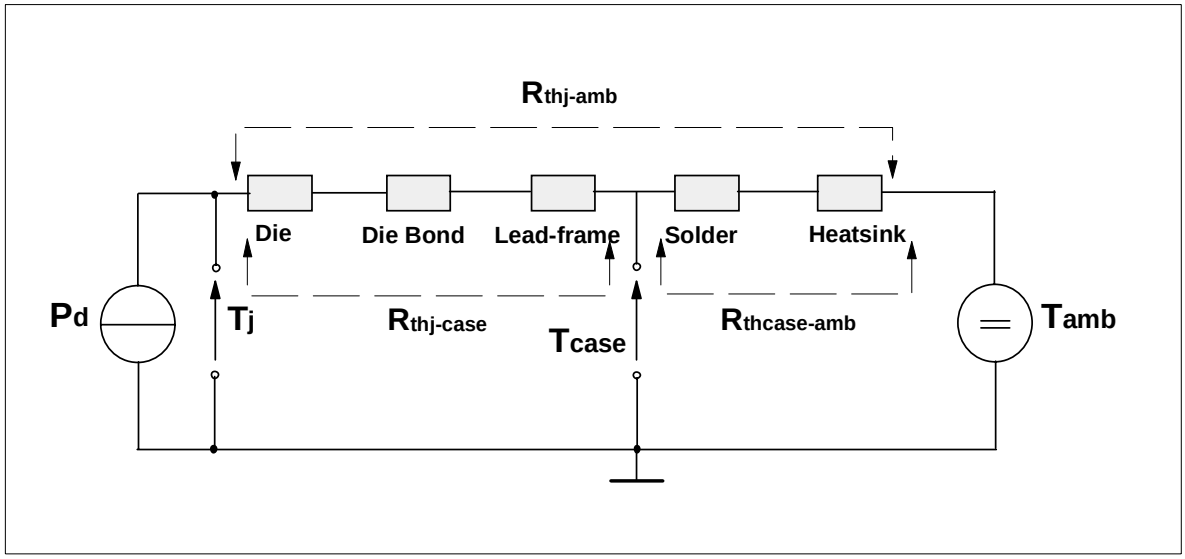
$$R_{DS(on)}(150°C) = \frac{T_J - T_{amb}}{I_{OUT}^2 \cdot R_{thj-amb}}$$

This is the maximum value of $R_{DS(on)}$ which can be chosen. The steady state on-resistance of HSDs is a function of the junction temperature and in the datasheet its value is given at 25°C and this is approximately doubled at 150°C. In some cases it may be convenient to use an HSD with a bigger $R_{DS(on)}$ in the same package. To still comply with the above equation we must reduce $R_{thi-amb}$ and have a better heatsink. The trend from through-hole packages to low-cost SMD applications has led to think of the PCB as a heatsink itself. In earlier packages (like PENTAWATT) a solid heatsink was either screwed or clamped to the power package and it was easy to calculate the thermal resistance from the geometry of the heatsink. In SMDs the heat path must be evaluated: chip (junction) - leadframe - case or pin - footprint - PCB materials - PCB volume - surroundings. To evaluate static thermal properties of an SMD an associated static equivalent circuit (see figure 4) can be considered. The power dissipation of the chip is symbolized by a current source whilst the ambient temperature is represented by a voltage source. By estimating the PCB heatsink area in a real application, the user can easily determine $R_{thj-amb}$ in still air,

which is the worst case; in real applications the values for the heat resistance are much lower. The following equation applies:

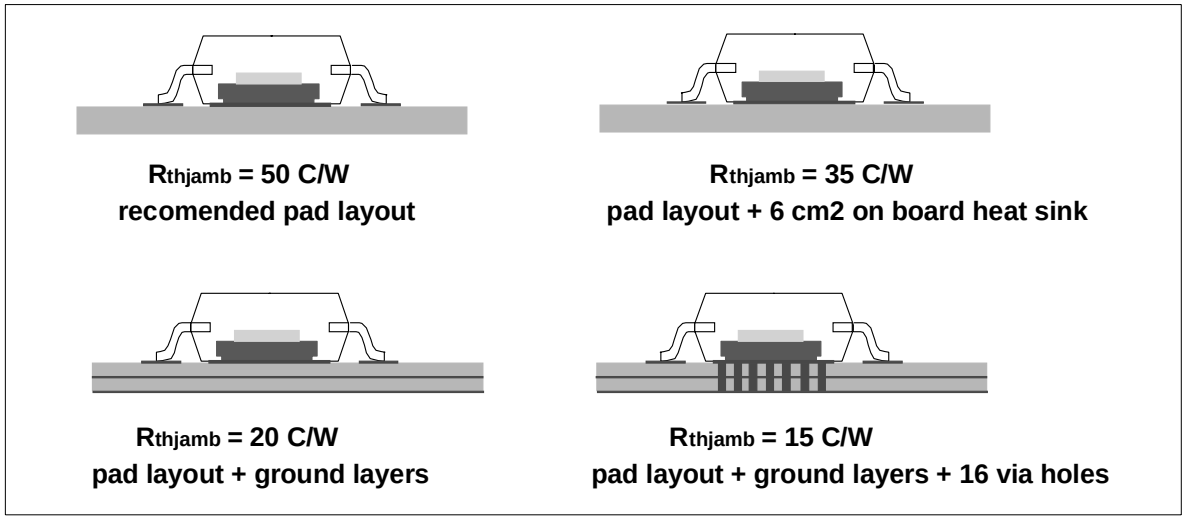
$$R_{thj-amb} = \frac{T_j - T_{amb}}{P_V}$$

Figure 4: Static thermal equivalent circuit



In the above equation, the power loss P_V and the ambient temperature T_{amb} can be easily determined in a temperature chamber. The chip temperature T_j can be derived during the operation, measuring the device's $R_{DS(on)} = (V_{CC} - V_{OUT})/I_{OUT}$.

Figure 5: PowerSO-10 recommended layout for high power dissipation capability

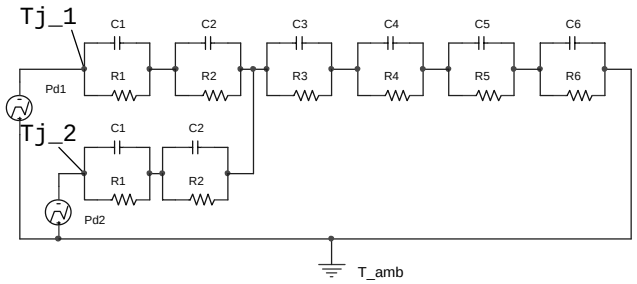


Having the characteristic $R_{DS(on)}$ versus T_j, the relevant chip temperature can be derived. Figure 5 shows different PCB layout for PowerSO-10 package. The thermal resistance $R_{thj\text{-}amb}$ can be reduced from 50°C/W to 15°C/W by holes linking different copper layers.

In the VIPower HSDs datasheets there are two sections concerning the thermal management. The first one shows the thermal calculation in order to find out the junction temperature in static conditions together with a plot of thermal resistance junction to ambient versus PCB heatsink area. The second one shows a plot of thermal impedance junction ambient in single pulse and the thermal model is shown with relevant thermal resistances and capacitors values (easy simulations can be performed both in static conditions and during transients as, for example, switching on a load with high in rush currents or PWM operation). In figure 6 an example of a double channel HSD thermal model is shown.

Figure 6: VND830 (SO16L package) thermal model

Area/island (cm^2)	Footprint	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.8	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	2.10E-03	
C3 (W.s/°C)	1.50E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	3	5



THE CONTROL AND PROTECTION CIRCUIT

Protection against low energy spikes and load dump

The voltage transients are very dangerous hazards to the automotive electronics. The transients tend to be either low energy- high voltage spikes or high energy-high voltage, up to 125V levels. The low energy spikes are generated by fast turnoff of high-current inductive loads, such as air-conditioning compressor clutches. This effect, combined with inductive behavior of wires, causes an overshoot voltage on the devices V_{CC} pin. M0-3 High Side Drivers have an internal protection designed to clamp the low energy spikes to 41V (V_{CC} clamp block in figure1). In this situation the energy can flow through the internal MOSFET T2 that is turned on through an internal clamp circuit (see figure 7).

M0-3 High Side Drivers are designed to successfully pass the 1, 2, 3a, 3b and 4 ISO-7637 standard pulses test (see table 1 carried in HSDs datasheets as well) - simulating the low energy voltage spikes. These values must be added to the voltage battery (for cars about 13.5V) to obtain the actual voltage. The N.5 ISO7637 pulse simulates the alternator load dump in the case of a Generator with an internal impedance of 2Ω and different values of magnetic field of the excitation circuit (see figure 8 for the level IV pulse); this occurs when the battery is disconnected whilst being charged by the alternator. The voltage spike can reach duration of approximately ½ second and it is of high-energy nature because of the alternator's low source impedance. Where a centralized clamp circuit is not provided or ISO7637 rated devices are not used, an external zener D_{ld} diode is necessary to clamp the transient voltage battery (see figure 7). This is done because an internal protection against load dump would require a larger die size and - therefore - higher cost than putting on a module level protection.

Figure7: V_{CC} clamp circuit against low energy spikes

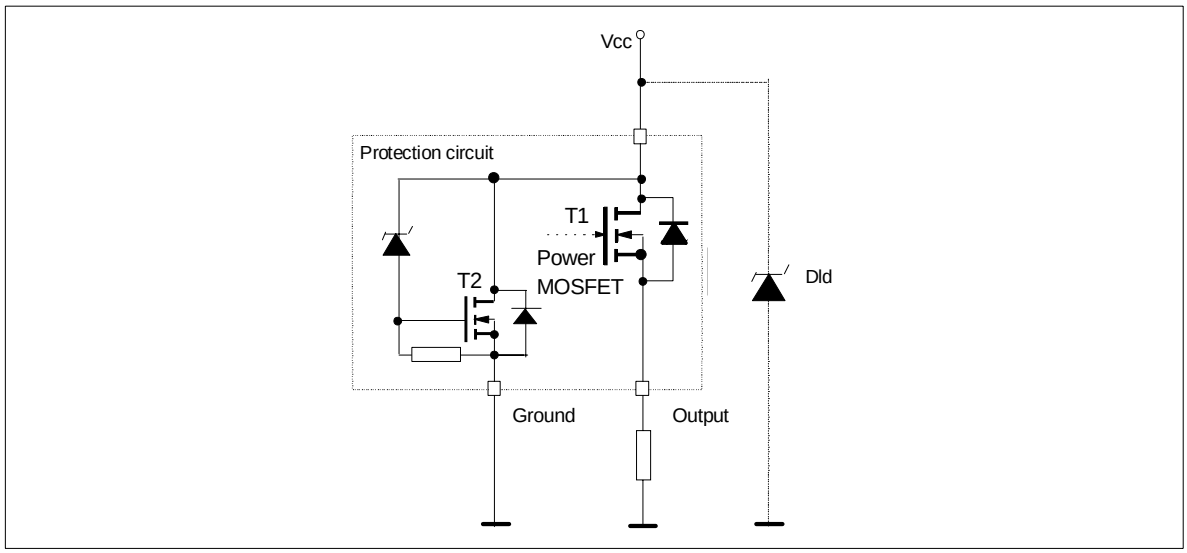
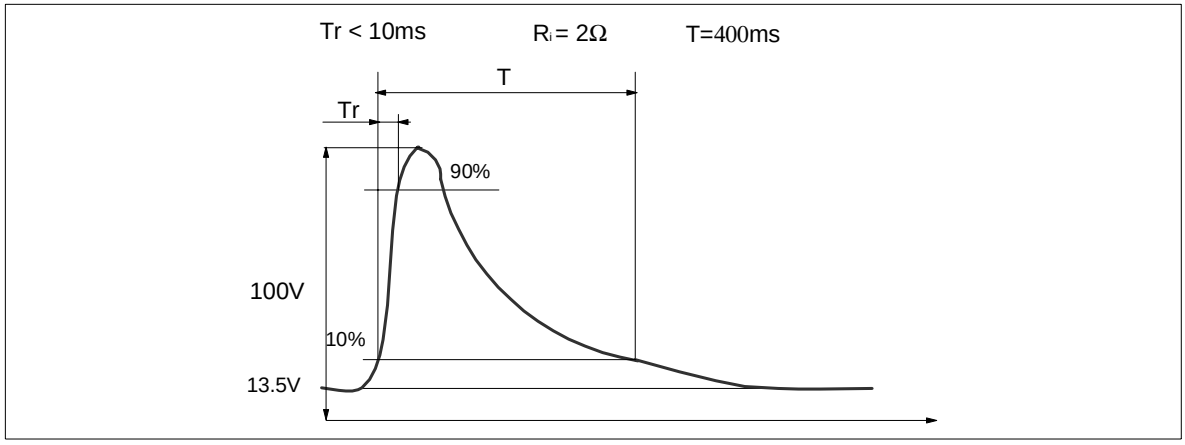


Table 1: Electrical transient requirements on V_{CC} PIN

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

Figure 8: N.5 ISO 7637 pulse (level IV)



Under and over voltage lockout

Under and overvoltage protections occur when the supply voltage drops or raises to minimum and maximum levels specified in the datasheet as V_{USD} and V_{OV}. Under V_{USD}=5.5V value the PowerMOS simply turns off, just because it would not work properly. The undervoltage condition may occur when turning on a car headlamp for example, which is a near short circuit. The inductive effect of wires (typically 1µH/m) generates an opposing voltage across the wire and the apparent supply voltage drops. The current increase rate for an HSD is about 1A/ms for a short-circuited load and using a 5m length wire, the induced voltage will not be large enough to reduce the supply voltage below 5.5V and - therefore - the HSD switches on. The overvoltage control circuit acts as a protection for the load against overvoltages (V_{OV}=36V and above that value the device switches off).

Reverse battery protection

Most auto manufacturers specify that any electronic device must be able to withstand a reverse battery connection. The exact magnitude of the reverse voltage requirement varies per manufacturer, but the worst case seems to be -24V for 10 min. The maximum allowed value of the ground current during reverse battery is $-I_{GND}$ and it is specified in the device's datasheet. There are two possible solutions to this problem.

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any kind of load. The following is an indication on how to dimension the R_{GND} resistor.

$$R_{GND} \leq 600mV / I_{S(on)\max} \quad (1)$$

$$R_{GND} \geq -V_{CC} / -I_{GND} \quad (2)$$

Power dissipation in R_{GND} during reverse battery situation is the following:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. In this case in the formula (1) $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices. When the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several HSDs sharing the same R_{GND}. This can lead to a very little value of R_{GND} to comply with formula (1) and formula (2) may not be fulfilled. To overcome this problem, ST suggests the following solution.

Solution 2: a diode (D_{GND}) in the ground line. A resistor (R_{GND}=1kΩ) should be inserted in parallel to DGND if the device drives an inductive load (see chapter about fast demagnetization). This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (~ 600mV) in the input threshold and in the status output values if the microcontroller ground is not common to the device ground. This shift will not vary if more than one HSD share the same diode/resistor network.

Micro-controller I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the HSD control pins will be pulled negative due to parasitic internal structures. This may cause the microcontroller I/O pins to latch up. The value of the resistors (R_{prot}) to be connected, is a compromise between the voltage shift from the micro-controller output to the HSD control pins, and the latch-up limit current of micro-controller I/Os. The following condition must be fulfilled:

$$\frac{-V_{CCpeak}}{I_{lu}} \leq R_{prot} \leq \frac{V_{out\mu C} - V_{IH} - V_{GND}}{I_{IN}}$$

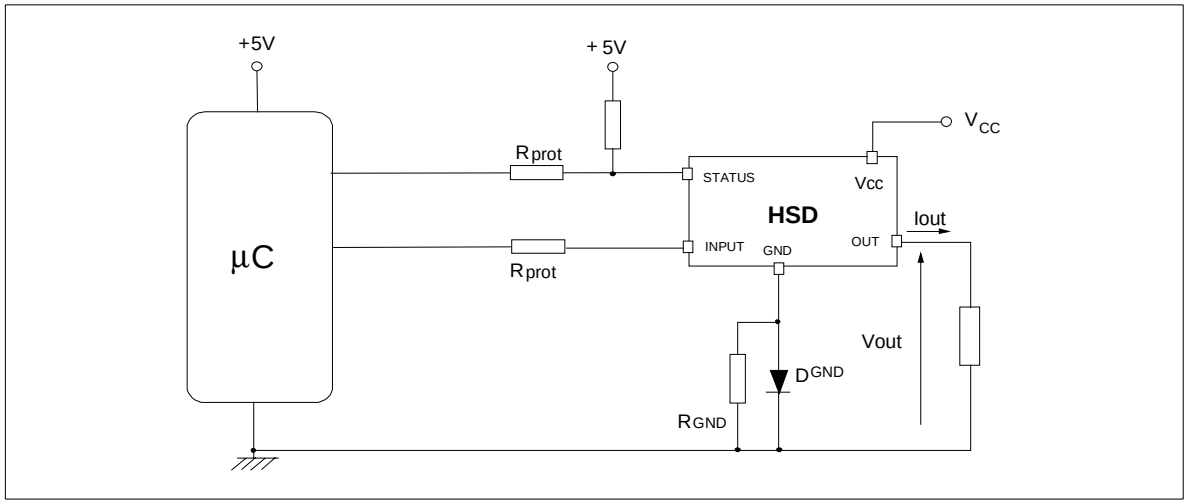
Where:

$-V_{ccpeak}$=negative peak voltage

I_{lu}=µC's latch up current
$V_{out\,\mu C}$=output µC's voltage
V_{IH}=minimum input HSD high level
V_{GND}=voltage drop across ground network
I_{IN}=maximum input current

Figure 9 shows the external circuitry used for reverse battery protection and micro-controller protection.

Figure 9: Ground and µC protection network



Over temperature protection

Over-temperature protection is based on sensing the chip temperature only. The location of the sensing element on the chip in the power stage area, ensures that accurate, very fast, temperature detection is achieved. The range within which over-temperature cutout occurs is T_{TSD}=150ºC minimum. The status output goes low with a maximum delay of only 20µs. Over-temperature protection acts to protect the device from thermal damage and limits the average current when short circuits occur in the load as well (see chapter about abnormal load conditions).

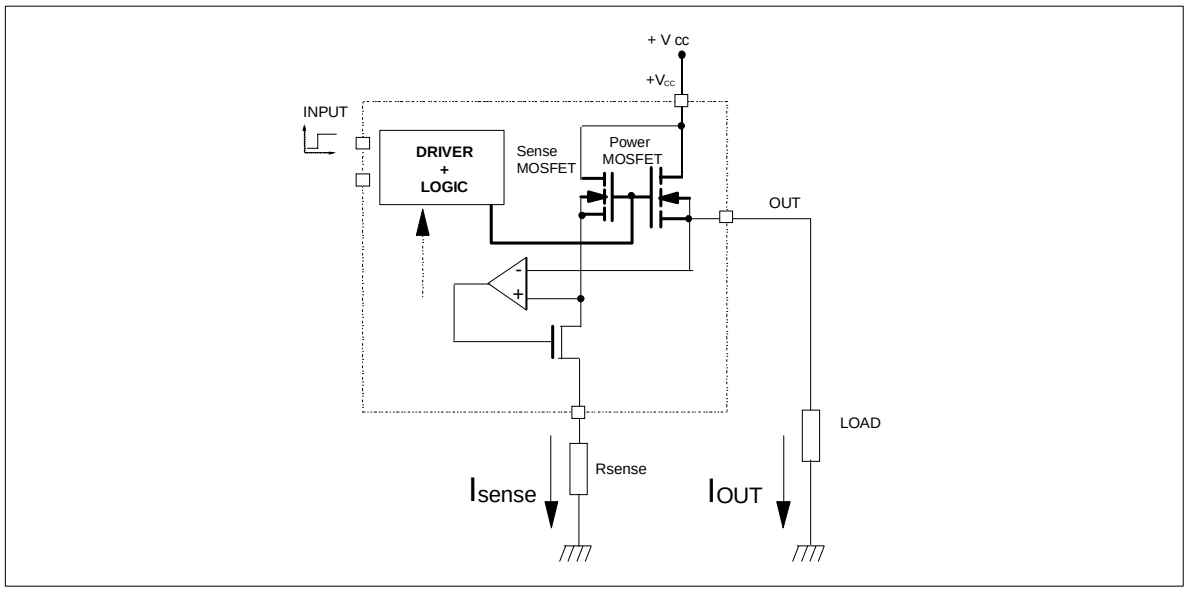
Analog current sense

Some of the new HSDs made by using the VIPower M0-3 technology have the current sense feature (VN60, VN61, VN92 and VNC6 lines). This allows to develop a voltage signal - that is proportional to the load current - across an external resistor R_{sense}. In figure 10 the HSD current sense circuit is shown. The principle of operation is to compare the currents flowing through two paths: the sense path made up of the series of n-cells PowerMOSFET plus the sense resistor (I_{sense}) and the power path made up of the series of N-cells MOS plus the connected load (I_{out}).

During the on-state condition the load current creates a voltage drop on the output pin; the OpAmp compares the voltage drop across the Power MOSFET $V_{dsN}=R_{DS(on)} \cdot I_{OUT}$ to the voltage drop across the n-sense MOSFET $V_{dsn}=R_{dsn} \cdot I_{sense}$; in normal operation $V_{dsn} = V_{dsN}$, therefore:

$$R_{dsn} \cdot I_{sense} = R_{DS(on)} \cdot I_{out} \qquad (3)$$

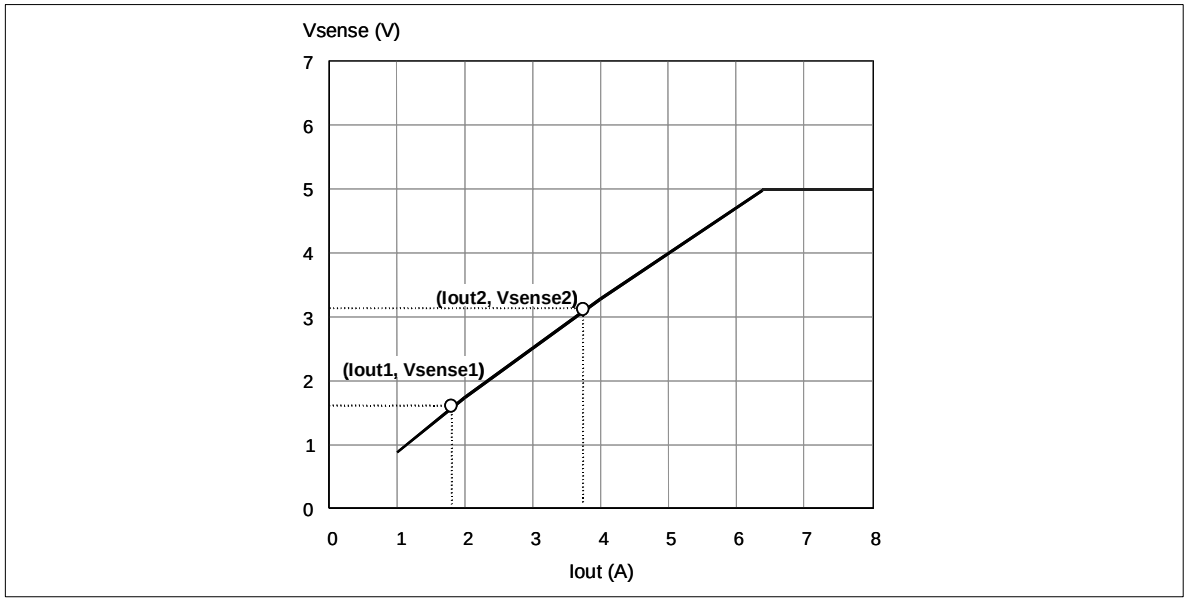
Figure 10: Current sensing internal circuit



Since V_{sense}=R_{sense} I_{sense}, putting K = R_{dsn}/$R_{DS(on)}$, this expression yields:

$$V_{sense} = R_{sense} \cdot I_{out} / K \qquad (4)$$

Figure 11: VN920 current sense plot and calibration points



The sense resistor is chosen applying formula (4) in order to have the desired voltage value to be read by the micro-controller A/D converter.

If a short circuit occurs and the device goes into thermal shutdown the sense voltage is pulled up at V_{SENSEH} value (given in the datasheets and typically 5.5V). The current sensing circuit has a maximum delay of 500µs. It is necessary to take into account that the K ratio may be influenced by some external and physical parameters like the resistance of the bonding wire that goes from the PowerMOS pad to the output pin R_K or the junction temperature and the battery voltage. For the VN92 family - for example - K spreads from 4400 to 5250 for a fixed I_{out}=10A and V_{sense}=4V in a temperature range from 25°C to 150°C. This application requires good sense accuracy, therefore it is necessary to decrease the K spread. When I_{out} is in the range 1.5 - 6.5A, the sense voltage is proportional to the load current (linear zone). The key method consists in fixing two load currents in the linear zone and measuring the relevant sense voltages. During the measurement T_{case}=25°C, R_{sense} is fixed and V_{CC}=13V. As explained before, given the output currents I_{out1} and I_{out2}:

$$V_{sense1} = \frac{R_{sense} \cdot I_{out1}}{K} \quad ; \quad V_{sense2} = \frac{R_{sense} \cdot I_{out2}}{K} \qquad (5)$$

The K ratio is the angular coefficient of the straight line to the two measured points (see figure 11). In the whole range of variation of the output current - we can suppose that:

$$I_{out} = K \cdot I_{sense} + b \qquad (6)$$

Thus:

$$I_{out1} = \frac{K \cdot V_{sense1}}{R_{sense}} + b \quad (7) \quad ; \quad I_{out2} = \frac{K \cdot V_{sense2}}{R_{sense}} + b \qquad (8)$$

In order to calculate "b" and "K" we can solve the system of two equations (7) and (8) with the fixed values of (I_{out1}, V_{sense1}) and (I_{out2}, V_{sense2}).

$$K = R_{sense} \cdot \frac{I_{ref2} - I_{ref1}}{V_{sense2} - V_{sense1}} \qquad (9)$$

$$b = R_{sense} \cdot \frac{I_{ref1} \cdot V_{sense2} - I_{ref2} \cdot V_{sense1}}{V_{sense2} - V_{sense1}} \qquad (10)$$

An easy algorithm can give us the "K" and "b" values. During the final test of a module, the two pairs (I_{out1}, V_{sense1}) and (I_{out2}, V_{sense2}) are stored in the relevant HSD microcontroller EEPROM. In this way the K ratio spread will be reduced of about 50%, even if the drift causes will still be present.

Open load detection (in ON and OFF state)

- Digital HSD

Open load detection occurs when the load becomes disconnected. The M0-3 HSDs can provide load disconnection detection during the off-state as well as in the on state. In digital HSDs, during the ON state a current IOUT flows through the power MOSFET (N cells MOS) and the load. The gate of a Sense MOSFET (n cells MOS) is driven at the same time and the correlation between the currents flowing in the two MOSFETs is the following:

$$I_{OUT} = \frac{N}{n} \cdot I_{senseMOS}$$

The internal circuit in figure 12 shows that if an open-load event occurs and the output current decreases below I_{OL}=K I_{REF} value the status voltage goes low, signaling a fault (for example, the minimum intervention threshold for VN75 is I_{OL}=50mA).

The open load detection during switching on, has a delay of 200µs, indicated on the datasheets as $t_{DOL(on)}$, whilst during ON state is zero. In the OFF state condition, the current doesn't flow through the power stage; in order to detect the open load fault, an external resistor is needed. In normal condition a certain current flows through the network made up of the pull-up resistor R_{pu} and the load (see figure 13)

and the voltage across is very low because the load resistance is supposed to be much lower than pull-up resistance. If this voltage stands below V_{OL} threshold, an internal comparator will keep the status pin in high impedence. If an open load occurs the output voltage is "pulled up" to a voltage close to the battery and more than V_{OL} value (maximum value 3.5V for M03 HSDs).

Figure 12: Open load detection in ON state for digital HSDs

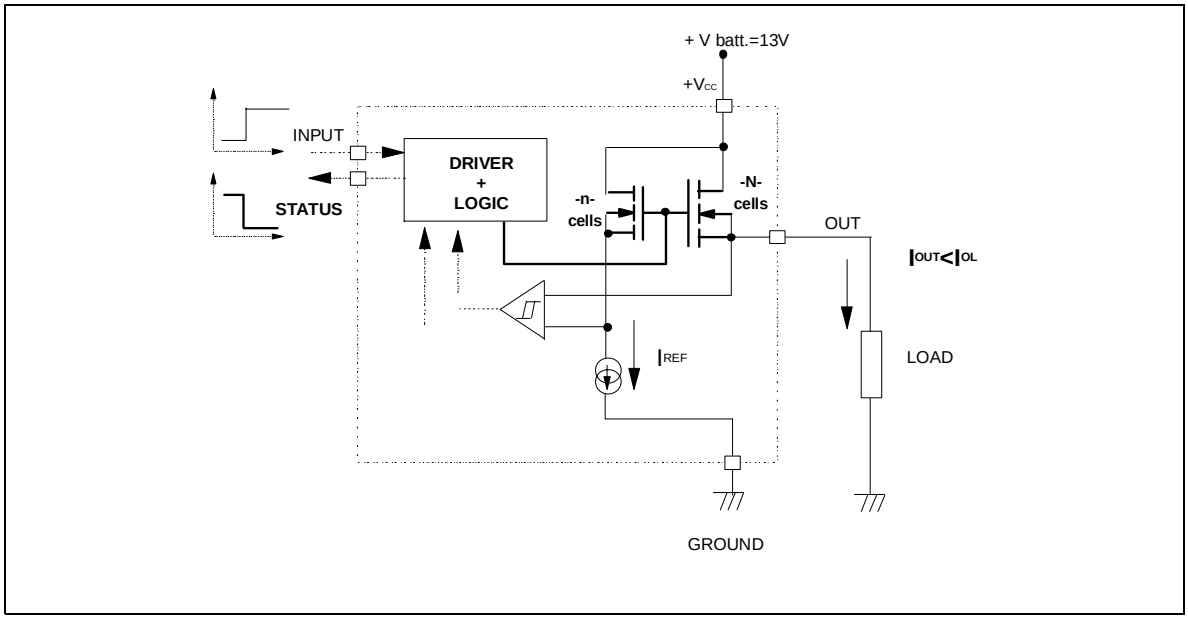
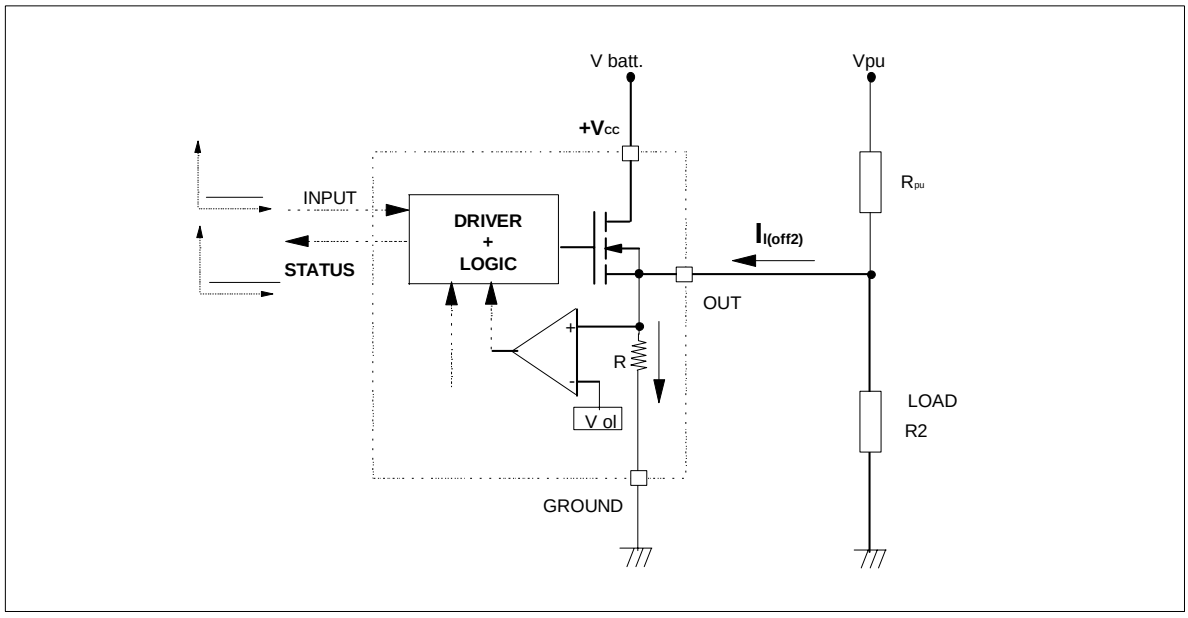


Figure 13: Open load detection in OFF state for digital HSDs



In the OFF state detection the delay is higher than the delay in the ON state (maximum $t_{DOL(on)}$=200µs and maximum $t_{DOL(off)}$=1ms).

The external pull-up resistor has to be selected according to the following requirements:

1) no false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin}; this results in the following condition:

$$V_{OUT} = \frac{V_{pu}}{R_L + R_{pu}} \cdot R_L < V_{OL\,\min}$$

2) no misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax}; this results in the following condition

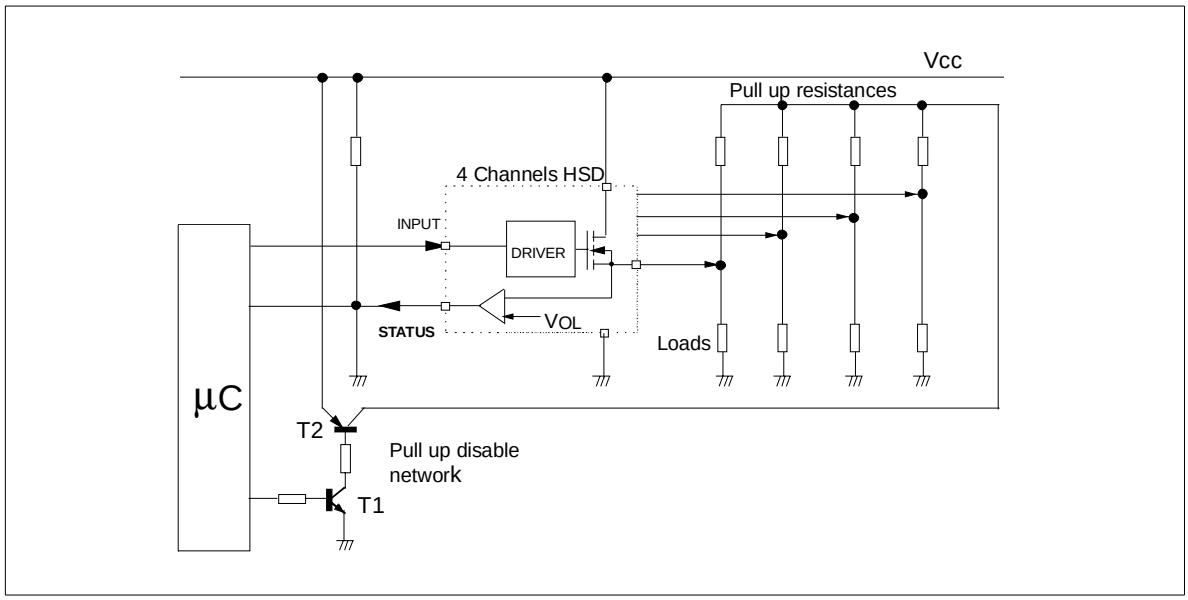
$$R_{pu} < \frac{V_{pu} - V_{OL\max}}{I_{L(off\,2)}}$$

The values of V_{Olmin}, V_{Olmax} and $I_{L(off2)}$ are available in the electrical characteristics section of datasheets. The need of the pull up resistor for any single HSD channel means power consumption even when the car is idle and a considerable increase of $I_{S(off)}$ parameter from a few µA to several mA. In order to avoid this, two ways can be chosen:

1) An external circuitry made of two transistors and two resistors.

Figure 14 shows a circuitry made of two transistors T1 and T2 connected in such a way that the collector of T2 drives all the pull-up resistors connected to different outputs of a four channels HSD (VNQ type). In this case the micro controller can simply check all the connected loads periodically for a very short time when the ignition key of the car is in. The bipolar transistors are cheap signal transistors.

Figure 14: Open load detection with external pull up network



2) A software trick for bulbs.

It is possible to detect an open load without connecting the pull-up resistor and without switching on the loads. This solution needs to implement some tricks by software. The Micro controller can periodically send a pulse to the input pin with a very short pulse width (for example 250µs). In this condition the HSD is switched on but the connected lamp cannot be heated up in such a short time. In addition the status

voltage can go low and signaling an open load condition (we remind that in ON state the status signal has a maximum delay of 200µs).

- Analog HSDs

In the previous chapter the current sense feature in M0-3 HSDs has been shown; this is active during the ON state only (INPUT=high) whilst in the OFF phase (INPUT=low) the current sense circuit is inactivated. This means that it is possible to detect an open load in ON state fault but not during OFF state. Two possible solutions can be thought of:

Solution 1: external comparator (see figure 15). Each load is connected to a pull up resistor supplied by the V_{CC} line through the network made of T1 and T2. The external comparator is needed to detect the voltage drop across the load and to compare it to a reference voltage (V_{ref} in the scheme). If an open load event occurs, the output pin voltage is pulled up to the V_{CC} value and the comparator provides the micro-controller with the fault signal. As seen for digital HSDs, the pull up disable network is supplied when the ignition key is in, but the car is off.

Solution 2: two additional signal bipolar transistor T3 and T4 can be used (see figure 16). The emitter of the T4 transistor (PNP type) is connected to a positive 5V line, and its base is connected to the HSD input line. This means that T4 is off when the HSD is on whilst it is on when the HSD is off. T3 (NPN type) collector is connected to the T4 one while T3 base to the output pin. T3 doesn't conduct until the output voltage (referred to ground) reaches its threshold value (V_{BE}). This is the case of normal condition in which the voltage drop on the load is almost zero.

When an open load fault occurs, the voltage on the input pin rises to the V_{CC} value. In this condition T3 conducts and a voltage of about 5V appears on the sense pin. Therefore the micro-controller will detect the open load fault in OFF mode.

Figure 15: Open load cicuitry for analog HSDs (OFF state) with an external comparator

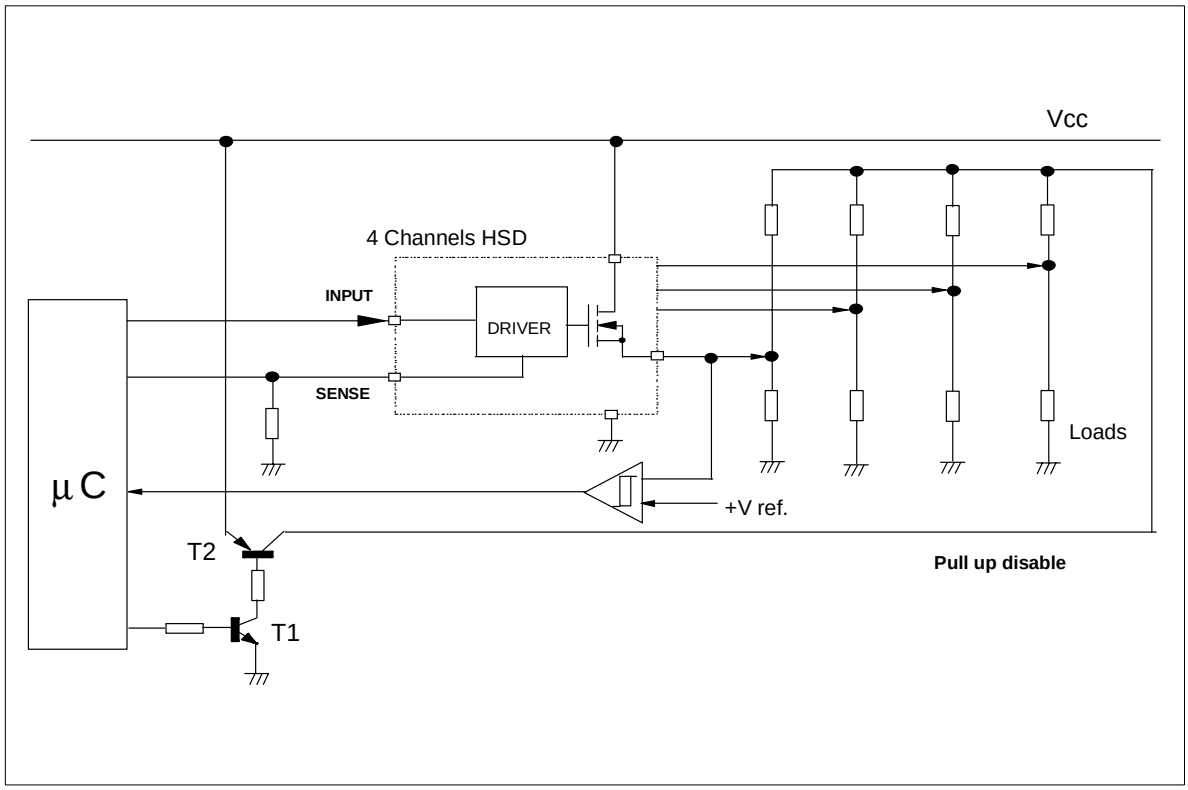
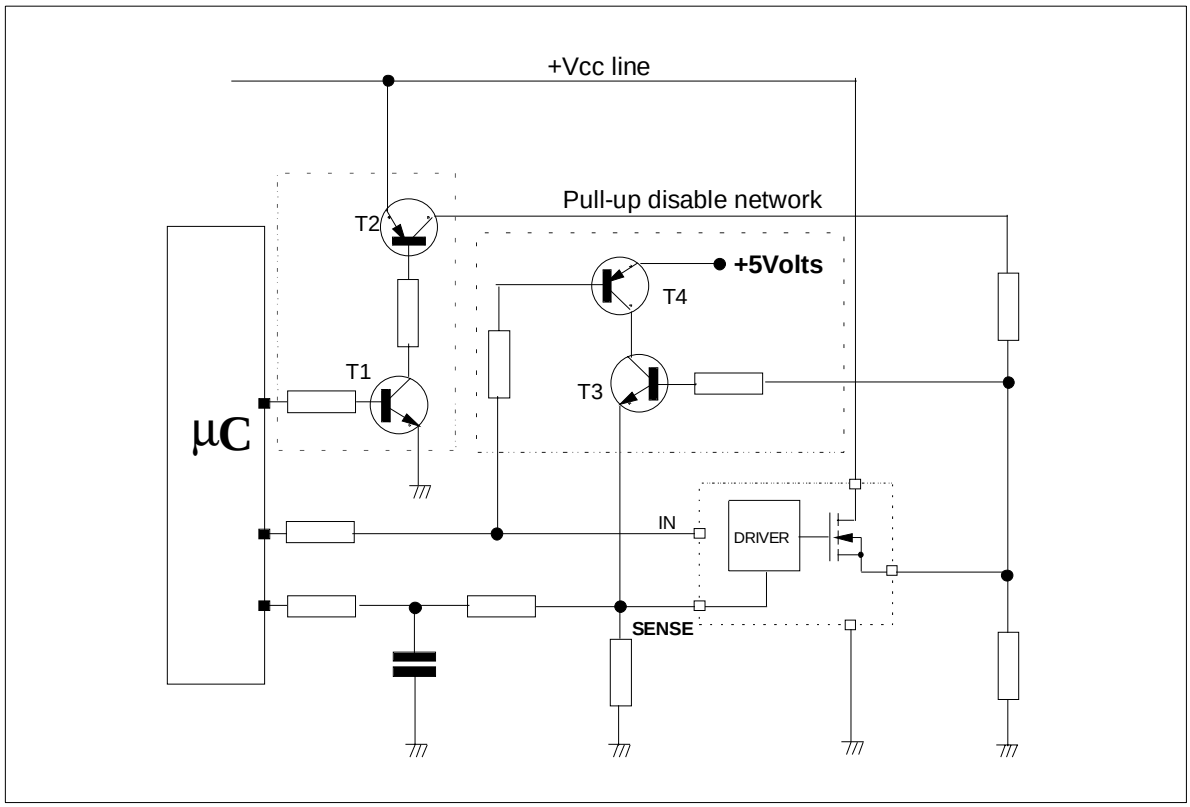


Figure 16: External circuitry for open load with two additional bipolar transistor T3 and T4



Voltage drop limitation feature

In the previous chapter, we highlighted the open load detection feature for High Side Drivers with digital diagnostic feature and analog current sensing as well. For digital ones, in the ON state condition an internal amplifier compares the voltage drop V_{DS} on the Power MOSFET due to the load current to the voltage drop on the internal Sense MOSFET (see figure 12). Its output drives a circuitry able to give an open load signal fault or a sense voltage across R_{SENSE} (analog HSD).

The High Side Drivers built by using the VIPower M0-2 technology (all with digital diagnostic), have a V_{DS} proportional to the load current (figure 17). This means that in the low output current range, the voltage between drain and source has the magnitude comparable to the amplifier offset (V_{offset}=5mV). Therefore the precision of open load detection becomes very low. At open load condition, the following equation can be written:

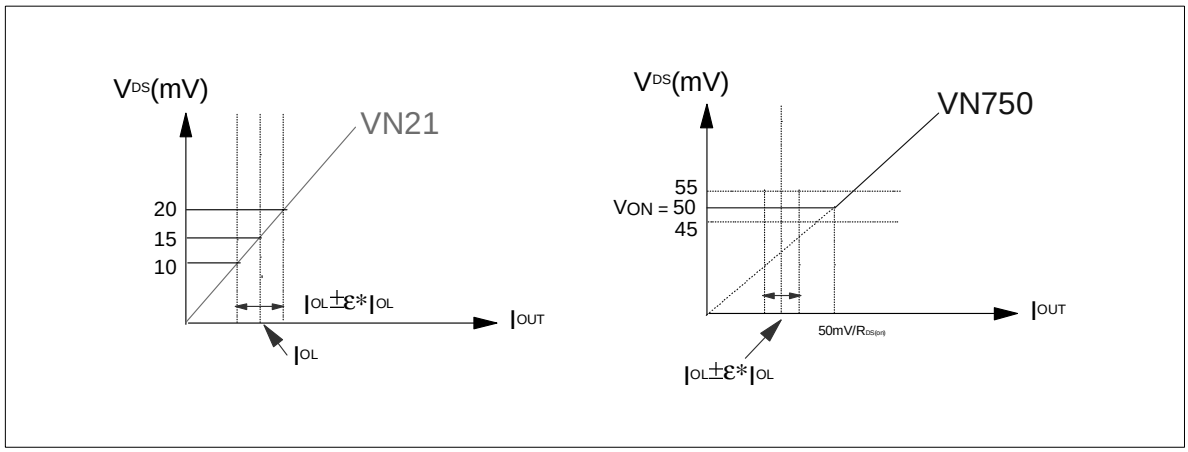
$$V_{CC} - R_{DS(on)} \cdot I_{OL} = V_{CC} - R_{senseMOS} \cdot I_{REF} \pm V_{offset}$$

$$R_{DS(on)} \cdot I_{OL} = R_{senseMOS} \cdot I_{REF} \mp V_{offset}$$

$$I_{OL} = \frac{R_{senseMOS}}{R_{DS(on)}} \cdot I_{REF} \mp \frac{V_{offset}}{R_{DS(on)}} = K \cdot I_{REF} \mp \frac{V_{offset}}{R_{DS(on)}}$$

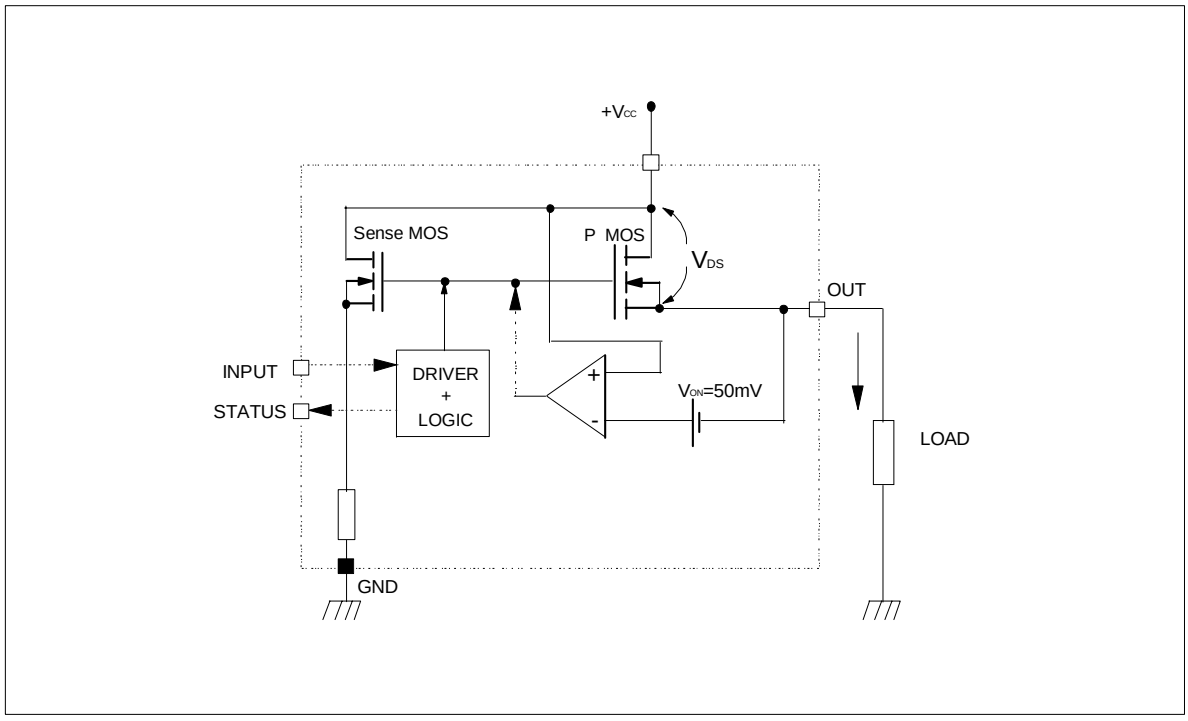
For example, let us consider an M0-2 HSD: VN21 with $R_{DS(on)}$=50mΩ, I_{OL}= K I_{REF}=0.3A (typical). The error on the voltage drop value due to the amplifier offset voltage is 5mV, and the formula (11) yields:

Figure 17: On resistance characteristics comparison between VN21 (M0-2) and VN750 (M0-3) HSDs



With a percentage error ε=33%. One of the advantages of the latest M0-3 digital HSDs, is the precision in the load current reading at low current value as well. This is achieved by driving the gates of the Power and Sense MOSFETs in such a way as to increase the on-state resistances of both of them at low load current. The diagram in figure 18 fulfills this feature; it is a feedback circuit: when I_{OUT} is low, and V_{DS} tends to be below V_{ON}=50mV, the internal amplifier allows the voltage gates (V_{GS}) to go low and therefore to increase the on resistances of both MOSFETs. Then V_{DS} goes up again to 50mV.

Figure 18: Voltage drop limitation circuit



The resistance of the Power MOSFET does not have a linear behavior anymore (see figure 17). It is increased to the value $R_{DS}=V_{ON}/I_{OUT} > R_{DS(on)}$. In this case, equation (11) becomes the following:

$$I_{OL} = \frac{R_{senseMOS}}{R_{DS}} \cdot I_{REF} \mp \frac{V_{offset}}{R_{DS}} = K \cdot I_{REF} \mp \frac{V_{offset}}{R_{DS}} \qquad (12)$$

K ratio remains constant while R_{DS} is increased. This allows a design that lowers the first addend of equation (12), that's to say the detection threshold. For example, the VN750, a M0-3 digital HSD with: $R_{DS(on)}$=60mΩ, is designed in order to have I_{OL}= K • I_{REF} at only 0.1A (typical).

At open load current the on state resistance R_{DS} of the Power MOSFET is the following (see figure 4):

$$R_{DS}=50mV/100mA=500m\Omega.$$

Much higher than the typical $R_{DS(ON)}$ value of 60mΩ. In this case, from eq. (12), the open load reading is the following:

$$I_{OL}=0.1A\pm5mV/500m\Omega=0.1\pm0.01A$$

- Analog HSDs

In case of HSDs with current sensing the behavior of open load detection is similar; the Power and the Sense MOSFETs are driven simultaneously in order to keep the differential signal above V_{offset}. The voltage drop limitation is V_{ON}=50mV too and is given in the protection section in the datasheets. The same equation (12) can be applied.

$$I_{OUT} = \frac{R_{senseMOS}}{R_{DS}} \cdot I_{sense} \mp \frac{V_{offset}}{R_{DS}}$$

Note that for HSDs (digital and analog) the precision of current reading depends on I_{REF} (I_{sense} for analog HSDs) and the ratio $K=I_{OUT}/I_{sense}= R_{senseMOS}/R_{DS(on)}$ as well.

Turn off of inductive loads (fast demagnetization)

When an HSD turns off an inductance a reverse potential appears across the load. The energy stored in the load during the ON condition has to be properly dissipated during switch off. The source of the Power MOSFET becomes more negative than the ground and this can reach the transistor's breakdown (see figure 19). To avoid this, the output has to be clamped at a certain demagnetization voltage, V_{demag}, of the specific inductance. In this condition the inductive load is demagnetized and its stored energy is dissipated internally in the HSD. In the basic HSD family the typical value of the demagnetization voltage is 4V. In the M0-3 HSDs the internal circuit clamps the voltage across the Power MOSFET to a typical value of 48V (given L=6mH, I_{OUT}=2A) and, therefore the voltage across the load is:

$$V_{demag} = V_{CC} - 48$$

In this condition the stored energy is removed rapidly in the Power MOSFET. The fast demagnetization leads to sudden junction temperature increase and, in case of repetitive pulses, this can cause chip and resin degradation.

If we suppose that the inductive load - which also has its resistance R_L - is switched off once it has reached the initial current I_0, the shape of discharge current during the switch off is given by:

$$i(t) = \frac{V_{demag}}{R_L} + I_O \cdot \left(1 - \frac{V_{demag}}{R_L \cdot I_O}\right) \cdot e^{-\frac{R_L}{L} \cdot t}$$

In the above equation, if we put i(t)=0, we can calculate the duration of demagnetization T_{demag}:

$$T_{demag} = \frac{L}{R_L} \cdot \ln\left(\frac{-V_{demag} + R_L \cdot I_O}{-V_{demag}}\right)$$

Figure 19: Switching off of an inductive load

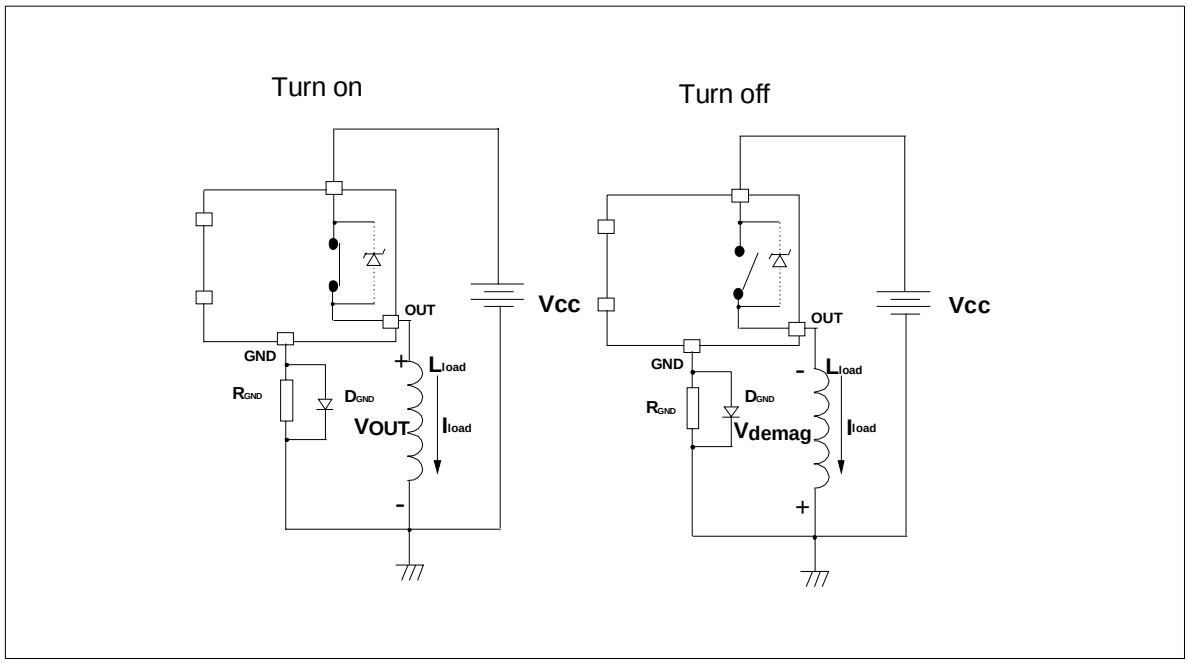
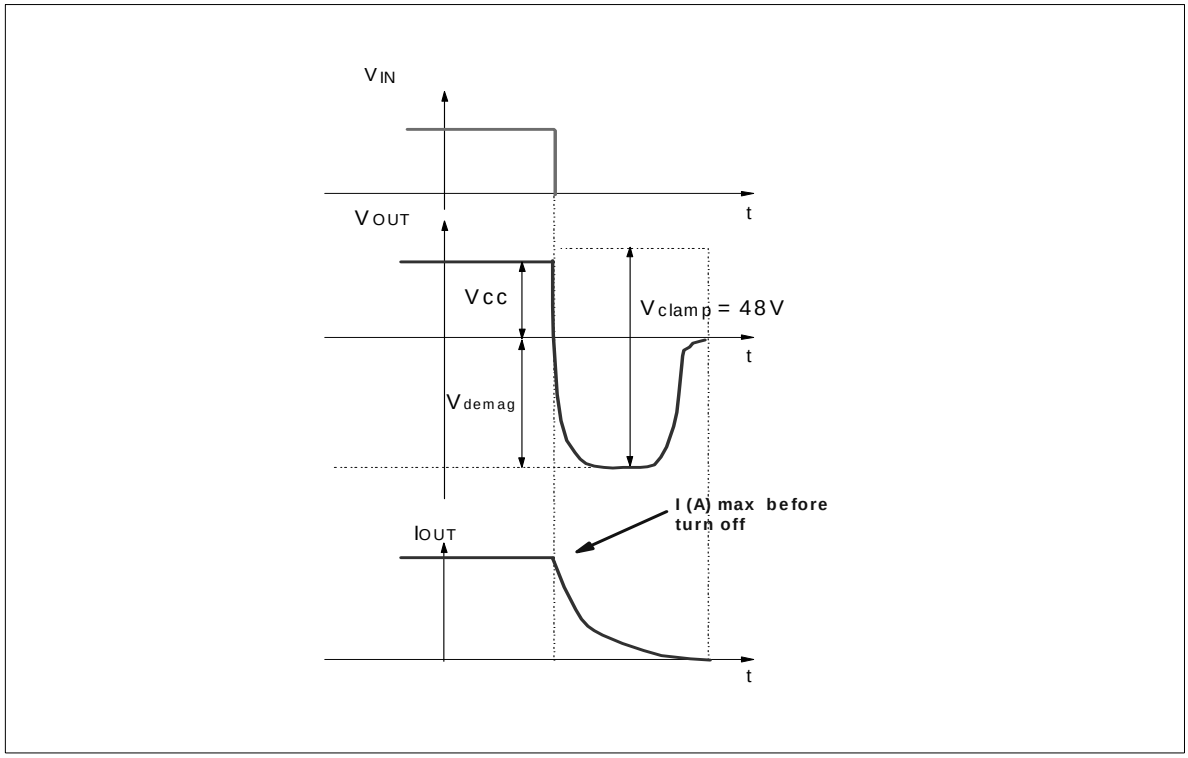


Figure 20: Waveforms of fast demagnetization



The faster we want to switch off, the bigger has to be V_{demag} compared with V_{CC}. The energy dissipated through the clamp circuitry during switch off is given by:

$$E_{demag} = \int_0^{T_{demag}} (V_{CC} - V_{demag}) \cdot i(t) \cdot dt = \int_0^{T_{demag}} (V_{CC} - V_{demag}) \cdot \left[\frac{V_{demag}}{R_L} + I_O \cdot \left(1 - \frac{V_{demag}}{R_L \cdot I_O} \right) \cdot e^{-\frac{R_L}{L} \cdot t} \right] dt =$$

$$\frac{-V_{demag} + V_{CC}}{R_L^{\,2}} \cdot L \cdot \left[R_L \cdot I_O + V_{demag} \ln \left(\frac{-V_{demag} + V_{CC}}{-V_{demag}} \right) \right]$$

The Power dissipated during turn off is:

$$P_{demag} = \frac{E_{demag}}{T_{demag}}$$

In case of repetitive pulses, the average power dissipated in the HSD is given by the following expression:

$$P_{av} = \delta \cdot P_{ON} + f \cdot E_{demag}$$

Where:

δ = duty cycle

f = frequency

P_{ON} = power dissipated during ON state.

When an external signal diode is used as reverse battery protection, an external resistor along with it connected to ground pin is necessary (see figure 19); in fact, during turnoff, the ground pin potential becomes negative in comparison with input voltage and this makes the Power MOSFET turn on again. Using R_{GND} (~ 1kΩ) the Ground pin potential is kept stable.

ABNORMAL LOAD CONDITIONS

Short circuit (start-up with the load short-circuited and short circuit occurring during on state)

When a load becomes short circuited, various effects occur and certain steps need to be taken to deal with them, particularly choosing the correct heat sink. Two clear cases of short circuit occur:

1)The load is shorted at start up

2)The load becomes short during the on state

At turn on the gate voltage is zero and begins to increase. Short circuit current starts to flow and power is dissipated in the HSD according to the formula:

$$P_d = V_{DS} \cdot I_{OUT} \cong V_{CC} \cdot I_{\lim}$$

The effect is to cause the silicon to heat up. The power MOSFET stays in the linear region. When the silicon temperature reaches a minimum temperature of 150°C, the over temperature detection operates and the switch is turned off. Passive cooling of the device occurs until the reset temperature is reached and the device turns back on again. The cycle is repetitive and stops when the power is removed, when the input is taken low or when the short circuit is removed. In this case the device controls the di/dt. Figure 21 shows a start up waveform when there is a short circuited load driven by a VN610SP. The initial peak current is 45A for this 10mΩ device. Note that the sense pin is at high impedance during limitation phase and is pulled up at about 5.5V during thermal shutdown. When a short circuit occurs during the on state, the power MOSFET gate is already at a high voltage, about V_{CC} +8V, so the gate is hard on. Hence the short circuit di/dt is higher than in the first case, and only controlled by the load itself. After the steady state thermal condition is reached, thermal cycling is the same as in the previous case. After a certain time from switching on, depending on thermal impedance of the device, the first thermal shutdown occurs. The

estimated junction temperature behavior versus time is shown in figure 22 for VN920SP with a current limitation range of 30A-50A with 45A typical value.

Figure 21: Automatic thermal cycle at start up

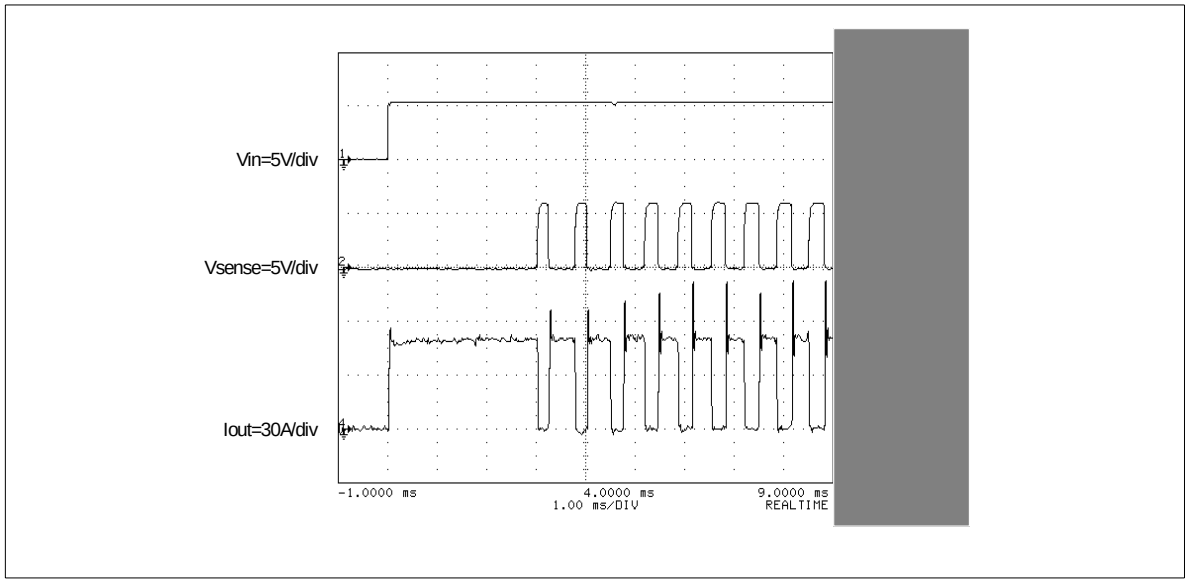
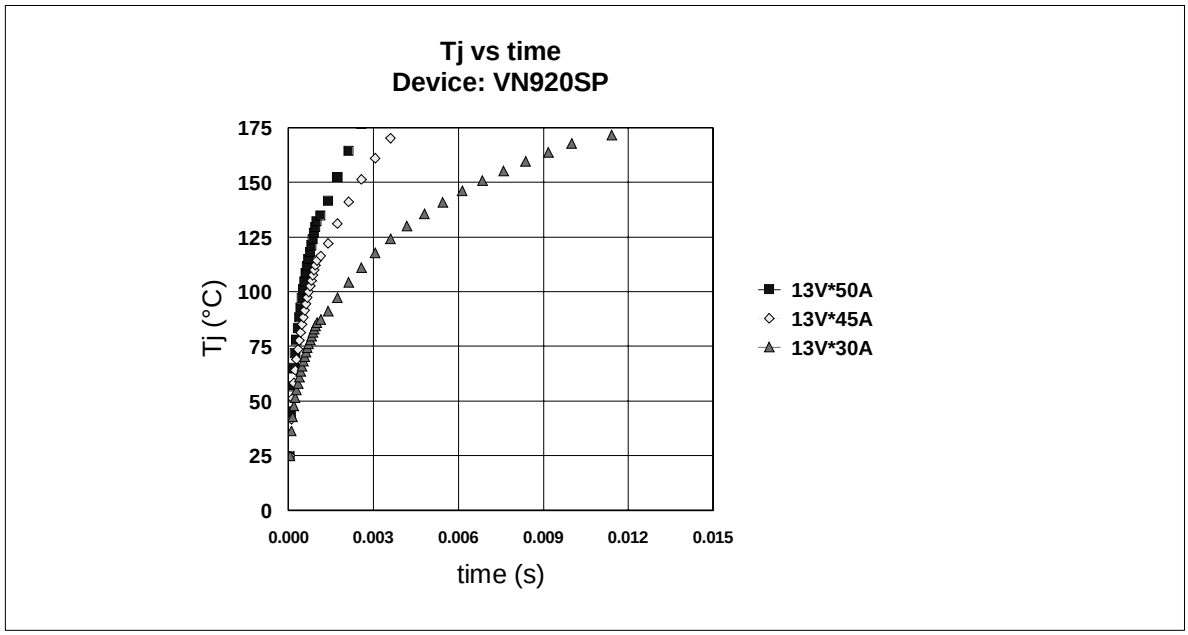


Figure 22: Junction temperature versus time for VN920SP on 2.5cm^2 FR4 70mm thick for minimum, typical and maximum limitation current



Obviously, when the maximum junction temperature is fixed, the higher the current limit, the faster the thermal shutdown intervention.

Evaluating the average and RMS currents in short circuit condition

The thermal cycling in overload conditions produces repetitive current peaks. The device switches on, the silicon heats up until the over-temperature sensing acts to turn the device off. The rate of passive cooling depends on the thermal capacity of the thermal environment. This, in turn, determines the length of the off state during thermal cycling.

It is important to evaluate the average and RMS current during short circuit conditions. This is required in order to determine the track dimensions for printed circuit boards. In all practical situations there is no danger to PCB tracks from these high peak current for tracks designed to handle the nominal load current. In steady state conditions the junction temperature oscillates between T_{TSD} (shutdown) and T_R (reset). The average temperature is:

$$T_{jav} = \frac{T_{TSD} + T_R}{2} \approx 168°C$$

If I_{AV} is the average current, the dissipated power is:

$$P_D = I_{AV} \cdot V_{CC}$$

Therefore - for a specific package (fixed $R_{thj\text{-}case}$) - we have:

$$I_{AV} = \frac{T_{jav} - T_{case}}{R_{thj-case} \cdot V_{CC}}$$

Example:

VN92 - with T_{case}=85°C, $R_{thj\text{-}case}$=1°C/W and V_{CC}=13V - has an average current:

I_{AV} = (168-85)/(1·13)= 6.38A

The RMS current I_{RMS}, generates heat in the copper track on PCB during short circuits.

$$I_{RMS} = \sqrt{\frac{1}{T} \cdot \int_0^T I^2(t) \cdot dt} = \sqrt{\frac{1}{T} \cdot I_{\lim}^2 \cdot t_{on}} = \sqrt{I_{\lim} \cdot I_{\lim} \cdot \frac{1}{T} t_{on}} = \sqrt{I_{\lim} \cdot I_{AV}}$$

The RMS current increases proportionally to the square root of the peak current (for example if peak current is doubled, RMS current increases of 40%). Schemes to limit the current do not decrease the RMS current significantly.

CONCLUSION

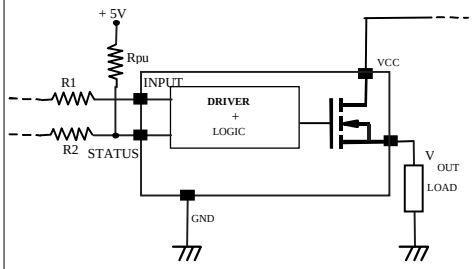
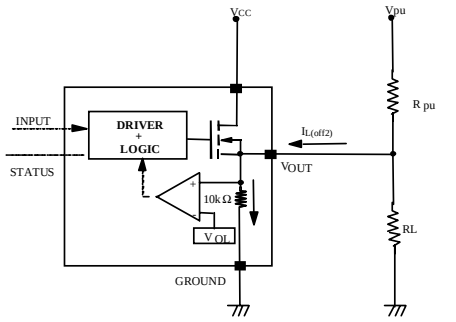
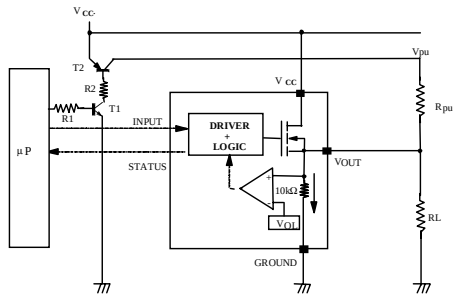
The new M0-3 High Side Drivers offer a reliable and cost effective solution versus electromechanical relays in automotive environment. They are versatile devices suitable for all power application in automotive: security, power train, light modules and body electronics. The option to use a selection of extra features such as digital or analogical diagnostic and current limitation, avoids to use external components like fuses that have to be replaced when a short-circuit occurs. In addiction every PCB track width must be adapted to the fuse. Another reason why use of VIPower HSDs is rapidly increasing is their great reliability if compared to electromechanical relays. In fact a standard number of cycles of a HSD is over 500,000 and the switching performance remains constant during lifetime. Every new generation of M0 technology has allowed to shrink die size and package footprint. The forthcoming M0-5, given the same load to be driven, will allow to halve the footprint area on board compared to M0-3. M0-5 together with smaller and cheaper SMD packages, will make feasible and near future scenario in which all mechanical switches will be replaced.

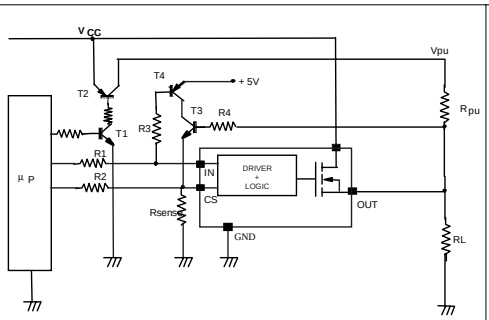
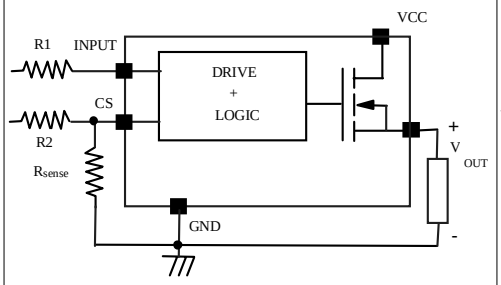
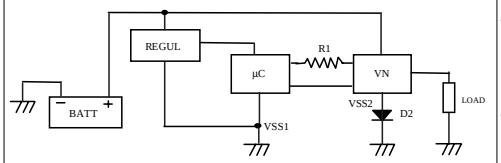
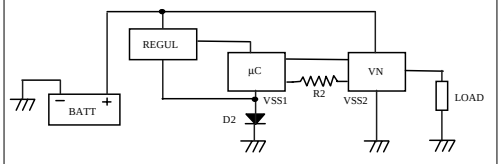
REFERENCES

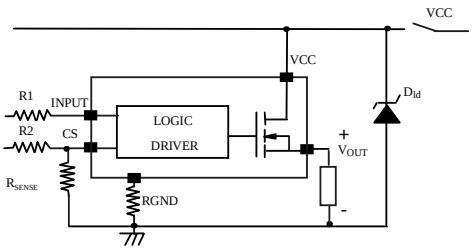
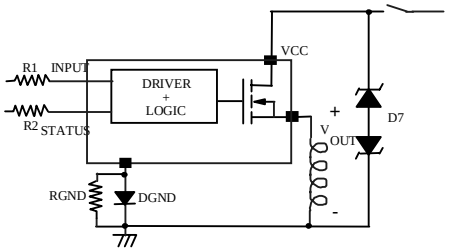
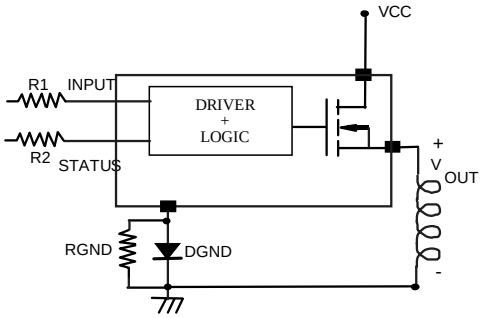
1) "*High Side Drivers*" A. Russo, B. Bancal, J. Eadie - SGS-THOMSON Application Note AN514/1092

2) "*How to Use the Advantages of VIPower in Automotive Lighting Systems*" R. Letor - Automotive Workshop - Rousset, May 23rd - 25th 2000

APPENDIX

	Symptom	Component	Schematic	Notes
1)	Input and Status pins	R1, R2, R_{pu}		R1, R2 and R_{pu} chosen in order to limit the control pins currents to 10mA. R1 and R2 must protect the microcontroller against the latch-up (see point 6, 7).
2)	Off-State open load detection in digital HSDs (case 1)	R_{pu}		Choose R_{pu} in order not to have false open load detection: $V_{OUT}=(V_{pu}/(R_L+R_{pu}))\bullet R_L<V_{OLmin}$ Choose R_{pu} to assure detection when load is disconnected: $R_{pu}<(V_{pu}-V_{OLmax})/I_{L(off2)}$ V_{OLmin}, V_{OLmax}, $I_{L(off2)}$ are given in datasheets.
3)	Off-State open load detection in digital HSDs (case 2)	R_{pu}, R1, R2, T1, T2		To minimize power consumption, the microcontroller can periodically switch on T1 and T2 when the ignition key is inserted.

4)	Off-state open load detection in analog HSDs	R1, R2, R3, R4, T1, T2, T3, T4		See point 3 - When open load event occurs a voltage of about 5V appears on CS pin.
5)	Current sensing (VN60, VN61, VN92, VNC6 lines)	R_{sense}		Choose R_{sense} in order to match V_{sense} with the micro analogic INPUT: $V_{sense}=R_{sense}$ I_{OUT} /K (see K parameter in datasheets)
6)	Ground potential differences (case 1)	R1, D2		V_{IL} and V_{IH} shifted by (V_{SS2}–V_{SS1}). R1 prevents the microcontroller to latch up, by limiting the input current under micro threshold current I_{lu}. $R1 > -V_{ccpeak}/I_{lu}$ $R1 < (V_{outµC} – V_{IH} –0.6V)/I_{IN}$
7)	Ground potential differences (case 2)	R2, D2		In fault conditions the device pulls the status pin down to V_{SS2} and the microcontroller sees a negative voltage – (V_{SS1}–V_{SS2}). Risk of microcontroller latch up: add R2 to limit the current. Undervoltage and offstate open load levels are not shifted.

8)	Load dump	D3 or RGND		External suppressor D_{ld} used for load dump > 40V. Alternative resistor R_{GND} can be added to the ground pin to limit the current in the control part in case it exceeds the signal path breakdown voltage
9)	Inductive loads: V_{CC} disconnection	D7		V_{CC} disconnection occurs each time the ignition key is turned off and if the load is highly inductive. If current is too high, the device could be destroyed. In some extreme cases, a 40V MOV (D7) is necessary.
10)	Inductive loads: GND pin pulled negative during switching off	R_{GND}		R_{GND} is necessary during fast demagnetization because it pulls down to zero the GND voltage. R_{GND} suggested value is 1kΩ.