AN1537
APPLICATION NOTE

A SIMPLE TRICK ENHANCES L5991's STANDBY FUNCTION

by C. Adragna and G. Gattavari

This application notes describes a simple technique that allows improving the Standby function of the advanced PWM controller L5991. The price to pay for that is the addition of just two resistors and two diodes, but the benefit brought in terms of no-load consumption in mains-operated converters is worth this small fee. The effectiveness of the improved Standby function will be proved and assessed on a couple of existing designs.

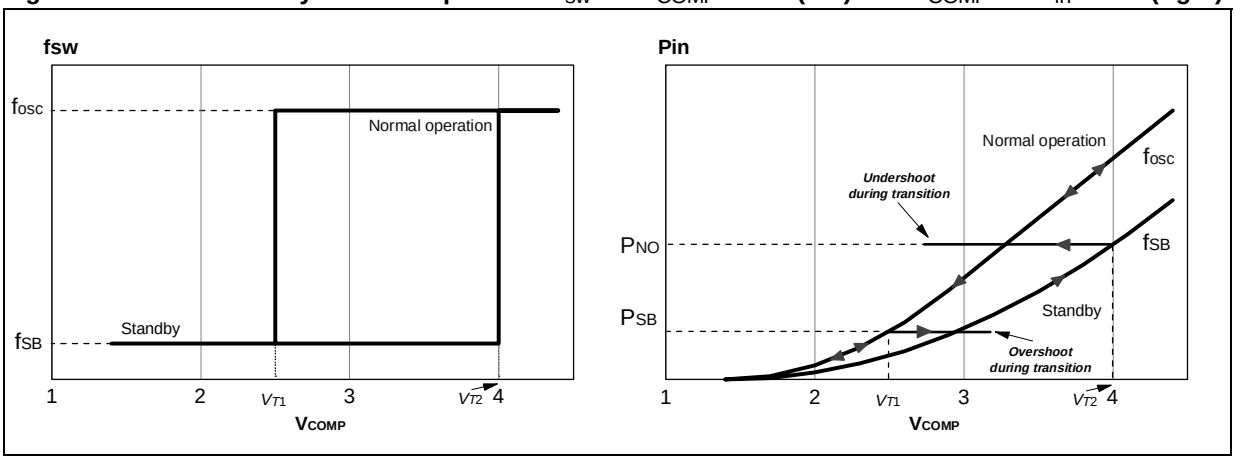
Introduction

L5991's Standby function is a valuable help in reducing light-load input consumption of offline converters and making them compliant with energy saving standards such as EnergyStar, Energy2000 and others. This function, optimized for flyback topology, is the ability of automatically - and abruptly - reducing the oscillator frequency (i.e. converter's switching frequency) as the converter's load falls below a defined threshold and restoring the normal oscillator frequency as the load increases and exceeds a second threshold.

The frequency shift allows minimizing power losses related to switching frequency, which represent most of losses at light or no load, without giving up the advantages of a higher switching frequency at full load.

Being the L5991 a current-mode controller [1], the output voltage (V_{COMP}) of its error amplifier (pin 6, COMP), except for an offset, is proportional to the peak primary current and then to the energy handled by the transformer cycle by cycle. It is then possible to deduce converter's load conditions by monitoring V_{COMP}.

Figure 1. L5991's Standby function operation: f_{sw} vs. V_{COMP} locus (left) and V_{COMP} vs. P_{in} locus (right).



If the peak primary current decreases as a result of a decrease of the power demanded by the load and V_{COMP} falls below a fixed threshold (V_{T1}), the oscillator frequency will be set at a lower value (f_{SB}). If now the peak primary current increases and V_{COMP} exceeds a second threshold ($V_{T2} > V_{T1}$) the oscillator frequency will be reset at the normal value (f_{osc}). Since the frequency shift causes V_{COMP} to shift too but in the opposite direction for energy balance reasons, an appropriate hysteresis (V_{T2}-V_{T1}) is provided to prevent the oscillator frequency from switching back and forth between f_{SB} and f_{osc}. This operation is shown in fig. 1.

The L5991 allows programming both the normal and the standby frequency. V_{T1} and V_{T2} are internally fixed but

it is possible to adjust the thresholds in terms of input power level (P_{NO}, P_{SB}) by adding a DC offset on its current sense input (pin 13, ISEN). Reference [2] provides plenty of details on this function and its usage.

There is a maximum abrupt frequency shift allowed, which is related to the amount of hysteresis: the theoretical maximum ratio of f_{osc} to f_{SB} is 5.59, however this value does not account for the dynamic changes of V_{COMP} during the transients resulting from the frequency shift. As a matter of fact, depending on the closed-loop characteristics of the voltage control loop and on the amplitude of the load change that causes the frequency shift, V_{COMP} may overshoot or undershoot before reaching its new steady-state value (see figure 1). If during a transient the other threshold is crossed, V_{COMP} may bounce from one threshold to the other and the switching frequency be unstable, going back and forth from one value to the other. As a result, the practical limit is less than the theoretical value, probably less than 4 and, at any rate, the control loop dynamics needs to be kept relatively slow to limit the aptitude of V_{COMP} to under- or overshooting.

In [2] it is explained also that the addition of a DC offset on the current sense pin increases the maximum f_{osc} to f_{SB} ratio allowed. However, this technique is suitable for allowing a higher f_{osc} with a given f_{SB}. The lower limit on f_{SB} is determined by other considerations: if it is in the audible range (< 16kHz), the transformer will very likely generate audible noise, especially at power levels where the frequency is about to shift back to f_{osc}, because of the high peak current involved.

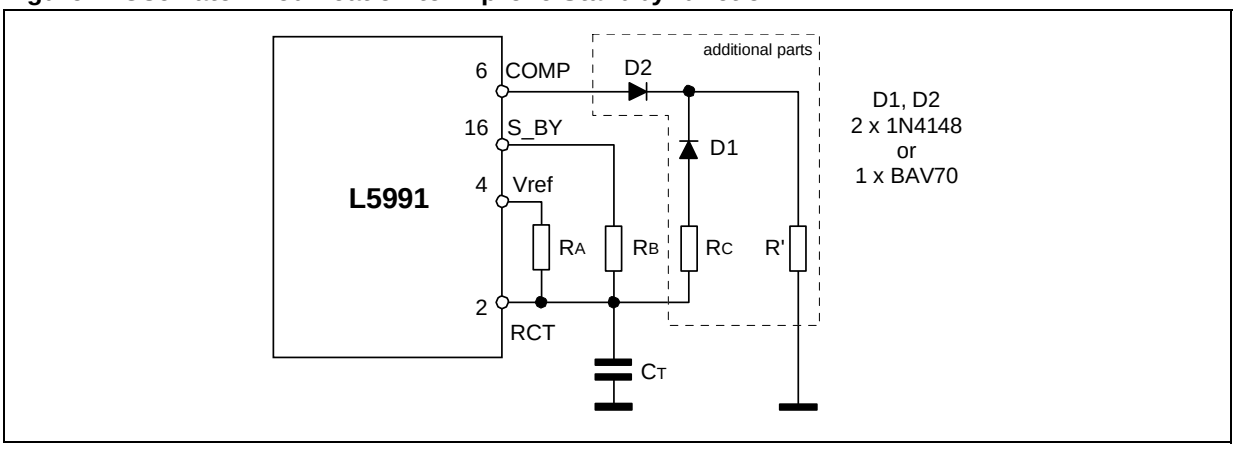
Often, instead, for a given f_{osc} an f_{SB} as low as possible would be required to meet the latest design targets aimed at complying even with the most severe energy saving standards. In this case it would be desirable to have a very low frequency under no-load conditions, where the peak current is too small to be able to generate audible noise, and a frequency above the audible range at power levels where audible noise issues may arise. This is exactly the purpose of the modification to the oscillator proposed in the following section.

Standby function improvement

To realize the aforementioned function, the oscillator frequency needs to be dependent on converter's load conditions - the lower the load, the lower the frequency and vice versa - and only when this is useful, that is at light load. This can be done by adding few parts to the oscillator of the L5991, as shown in figure 2.

Assuming a perfect matching of the two diodes (with a common-cathode dual diode like the BAV70 this is closer to reality), when V_{COMP} falls below 3V (oscillator's peak voltage) some of the current that charges C_T is diverted to ground through R_C, D1 an R'. In this way the rate of rise of the voltage across C_T is slowed down and the oscillator frequency decreased, the lower V_{COMP} the lower the frequency. Instead, when V_{COMP} is greater than 3V D1 isolates R_C and the oscillator frequency will be either f_{osc} or f_{SB}, like in the standard L5991 oscillator circuit. R_A, R_B and C_T can be then calculated as usual with the formulae given in [1]; as to the determination of R_C and R' please refer to the appendix.

Figure 2. Oscillator modification to improve Standby function



D2 compensates for the temperature shift of the forward voltage drop V_F of D1. Considering that the current flowing through the diodes is in the hundred µA or less, D1 and D2 dissipate negligible power and only ambient temperature affects their V_F. Assuming D1 and D2 match perfectly, neither oscillator frequency nor the point where R_C comes into play will depend on ambient temperature. In real-world operation, considering also that D1 and D2 do not usually carry the same current, a minimum temperature effect can be observed.

The "frequency foldback" provided by the additional circuit starts in the neighborhood of V_{COMP} = 3V, that is a little before that the high-to-low frequency shift takes place. After the shift, V_{COMP} will be higher and then the switching frequency will be close or exactly equal to f_{SB}, depending on the f_{osc} to f_{SB} ratio.

In applications where the switching frequency needs not be tightly fixed for some specific reason there is no major drawback to this technique. The only point to take care of is that the oscillator frequency be in the audible range only when the peak current is so low that no sound may come from the transformer, even when it is made with normal construction techniques. This can be obtained simply by choosing f_{SB} well above the audible range (e.g. f_{SB} > 30kHz seems to be a good rule of thumb).

The benefits, on the contrary, are considerable:

1) Very low switching frequencies are possible which, as already stated, will allow treating the power throughput as much efficiently as possible: MOSFET's capacitive losses, gate drive consumption and other parasitic losses will be minimized. See [2] for more details on them.
2) Since the additional components will be concerned with taking the oscillator frequency to very low values, the standby frequency f_{SB} can be kept relatively high, thus reducing the abrupt frequency shift and eliminating the need for a slow feedback to prevent frequency instability. As already said, keeping f_{SB} high has the positive side-effect of eliminating audible noise issues.
3) As a result of the faster dynamic response, start-up under no-load conditions is possible even with a minimum pre-load on the output. The dummy load represented by the feedback network, as well as bleeders, if used, can be minimized. The limit to the dummy load reduction is given by the collapse that the voltage delivered by the self-supply winding experiences with no load, which must not pull the supply voltage of the L5991 below the UVLO threshold.

To evaluate how much this function modification improves converter's performance at light or no load, the 45W wide-range mains AC-DC adapter illustrated in [3] and the 80W power-factor-corrected AC-DC adapter described in [4] will be optimized following the guidelines revealed by the above considerations. The "European Code of Conduct on Efficiency of External Power Supplies", ECC in short, whose limits are summarized in table 1, will be assumed as the reference.

Table 1. Limits envisaged by European Code of Conduct on Efficiency of External Power Supplies

Rated Input Power	Max. no-load Power Consumption		
	Phase 1 01.01.2001	Phase 2 01.01.2003	Phase 3 01.01.2005
≥ 0.3W and < 15W	1.0W	0.75W	0.30W
≥ 15W and < 50W	1.0W	0.75W	0.50W
≥ 50W and < 75W	1.0W	0.75W	0.75W

Optimization of a 45W, wide-range mains AC-DC adapter

For reader's convenience, table 2 summarizes the electrical spec of the adapter under consideration. Please refer to [3] for a detailed description and full evaluation data.

Table 2. 45W, wide-range mains AC-DC adapter: electrical specification of the original design

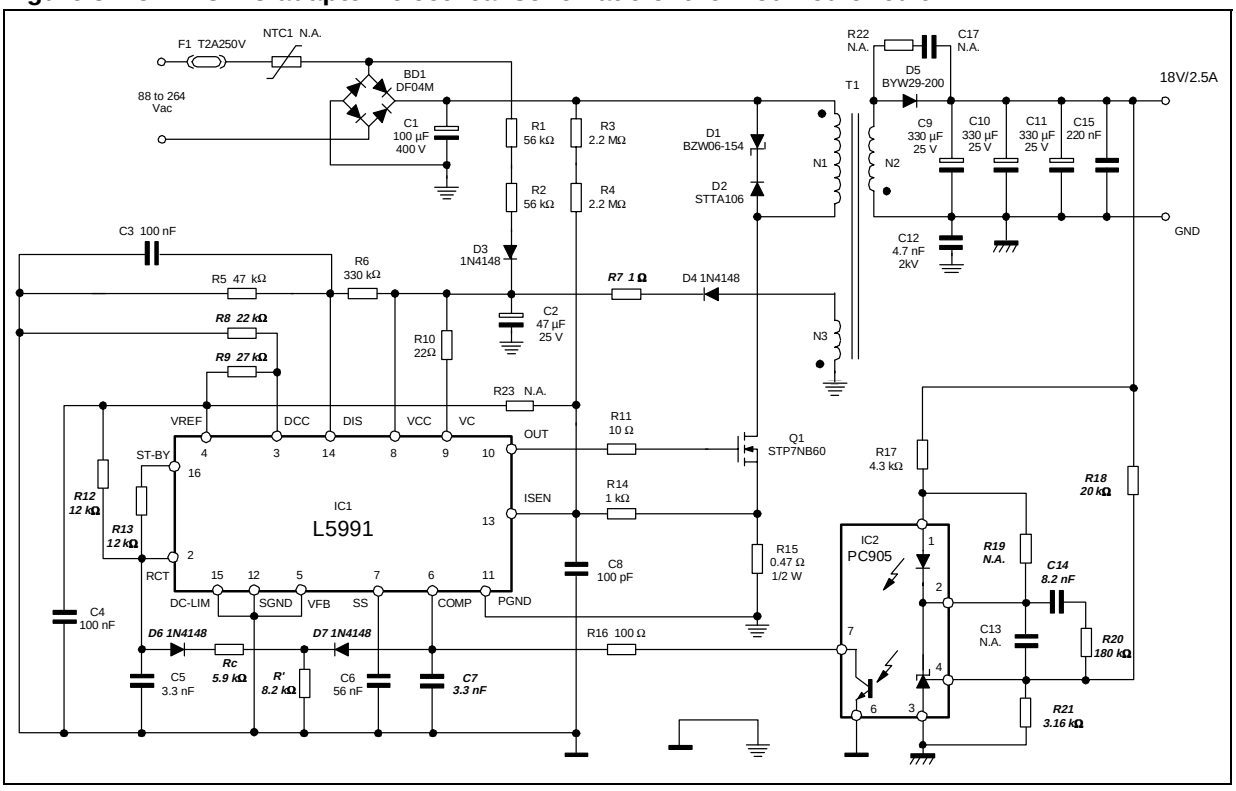
Input Voltage Range (V_{in})	88 to 264 Vac
Mains Frequency (f_L)	50/60Hz
Maximum Output Power (P_{out})	45W
Output	Vout = 18V ± 3%
	Iout = 2.5A max.
	Full load ripple ≤ 2% pk-pk
Normal Operation Switching Frequency (f_{osc})	70kHz typ.
Light Load Switching Frequency (f_{SB})	18kHz typ.
Full-load Efficiency (@ Pout =45W, Vin = 88÷264Vac)	> 80%
Maximum no-load Input Power (Vin = 88÷264Vac)	< 1W

Since the full-load input power is greater than 50W, this adapter belongs to the third bracket envisaged by the ECC. Its no load consumption is 0.9W @264Vac and 0.7W @220Vac then it meets Phase 1 limit (1W) and is close to that of Phase 2 and 3 (0.75W) with almost no margin.

Although the ECC specifies that the compliance test be done at the nominal voltage 230 Vac, in the pre-compliance test it is quite usual to refer to the consumption at 264 Vac, to account for production spread. With this criterion the adapter cannot be considered compliant with Phase 2 or 3 limits.

The target of the optimization is then to make the adapter ECC-compliant in the above mentioned sense. Figure 3 shows the electrical schematic of the converter with the added and modified components highlighted. Only these changes will be discussed.

Figure 3. 45W AC-DC adapter: electrical schematic of the modified circuit



1) The oscillator has been modified to maintain the same frequency under normal operation (70kHz) at full load and have a standby frequency equal to half the normal frequency (35kHz). The oscillator frequency with no-load will be 5kHz. Further details on the calculations can be found in the appendix.
2) The dummy load represented by the feedback components on the secondary side (170mW in the original design) has been reduced at 40mW: R21 has been increased from 348 Ω to 3.16kΩ and, consequently, R18 from 2.2 to 20kΩ to maintain the same regulated output voltage. This reduces the current consumption of the divider from 7.2 to 0.8mA. Additionally, R19 which was to provide 1mA extra bias current to the reference of the PC905, has been taken out since it was not strictly necessary.
3) The frequency compensation of the voltage control loop (C7, C14, R20) has been modified so as to get a larger bandwidth - it has been almost doubled - and then a faster response. The main purpose of that is to allow a correct start-up of the converter even with no load, whereas a slow feedback (basically, a large C14) causes the system to try continuously to restart under these conditions.
4) R7 has been decreased from 4.7 to 1 Ω, to prevent the supply voltage of the L5991 from going below the UVLO threshold with no load. To help this, the total consumption of the IC has been reduced by 0.3 mA by increasing R8 and R9 (from 5.6 to 22k Ω and from 6.8 to 27kΩ, respectively). Although with this change the voltage generated at full load is higher, it is still below the OVP threshold, set by R5 and R6, with a safe margin.

These modifications are summarized in table 3.

Table 3. 45W, wide-range mains AC-DC adapter: list of modifications to the original design

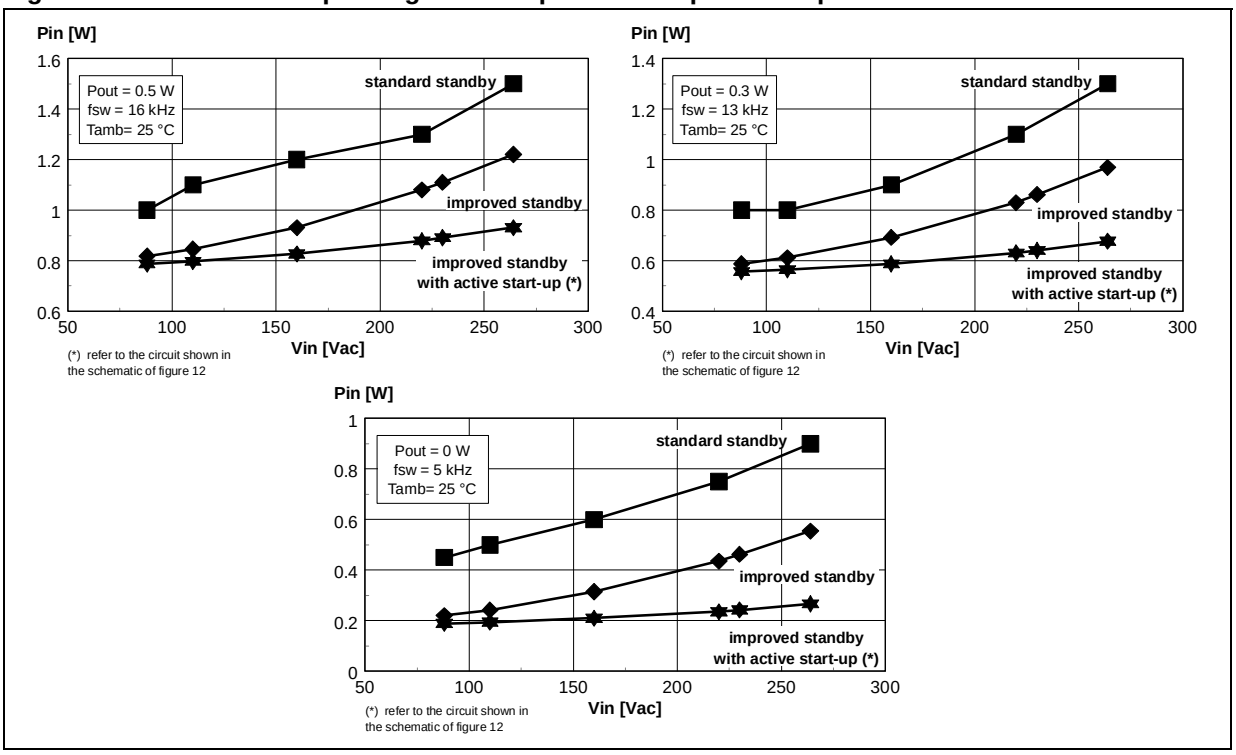
Part	Original value	New Value	Part	Original value	New Value
R7	4.7Ω	1Ω	R20	5.6kΩ	180kΩ
R8	5.6kΩ	22kΩ	R21	348Ω	3.16kΩ
R19	6.8kΩ	27kΩ	R_C	---	5.9kΩ
R12	24kΩ	12kΩ	R'	---	8.2kΩ
R13	8.2kΩ	12kΩ	C7	220pF	3.3nF
R18	2.2kΩ	20kΩ	C14	470nF	4.7nF
R19	1.2kΩ	---	D6, D7	---	1N4148

45W AC-DC adapter: evaluation results

The following diagrams compare the performance of the original design ("standard standby") with that of the modified one ("improved standby"). For reference, it has also been measured the input consumption after replacing the start-up circuit made up of R1, R2 and D3 with an active start-up circuit (see fig. 12).

To be noted in figure 4, the no-load consumption is < 0.6W @ 264Vac, then the adapter under test meets the ECC limits, Phase 3 (< 0.75W @230Vac) with some margin even without the use of an active start-up circuit.

Figure 4. 45W AC-DC adapter: light load input consumption comparison



The diagram on the left in figure 5 shows the relationship between output current and switching frequency obtained with the modified oscillator. The oscillator frequency is not much affected by the input voltage, as shown also by the oscilloscope diagrams of figures 6 to 10: the internal propagation delay of the current sense pin is compensated by R3 and R4, then the changes of V_{COMP} (and, consequently, f_{sw}) with the input voltage are negligible.

The diagram on the right in figure 5 illustrates the effect of temperature on both the oscillator frequency and the no-load input consumption (@264Vac) in the temperature range 0-70°C: the variation is very limited.

Figure 5. 45W AC-DC adapter: f_{sw} vs. I_{out} (left); P_{in} (@ P_{out} = 0) and f_{sw} vs. ambient temperature (right)

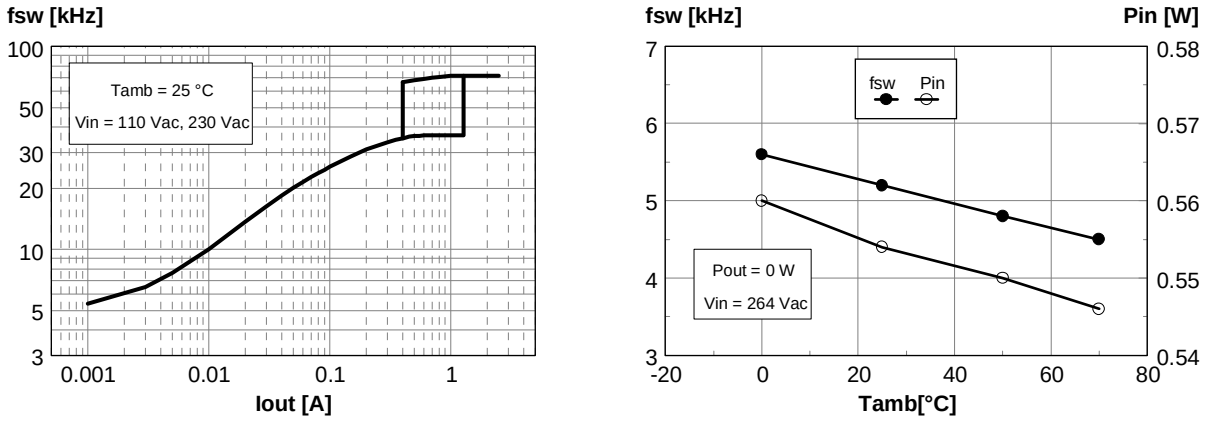
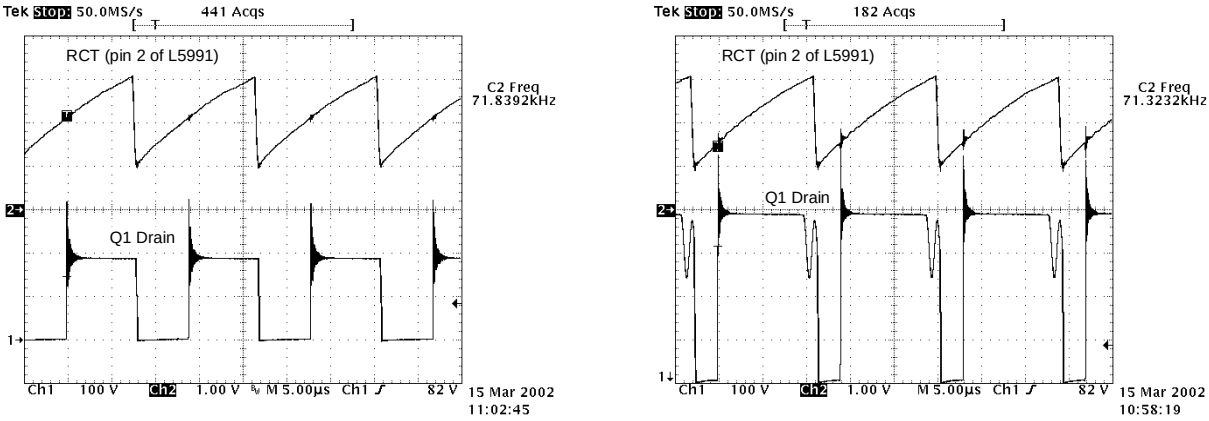


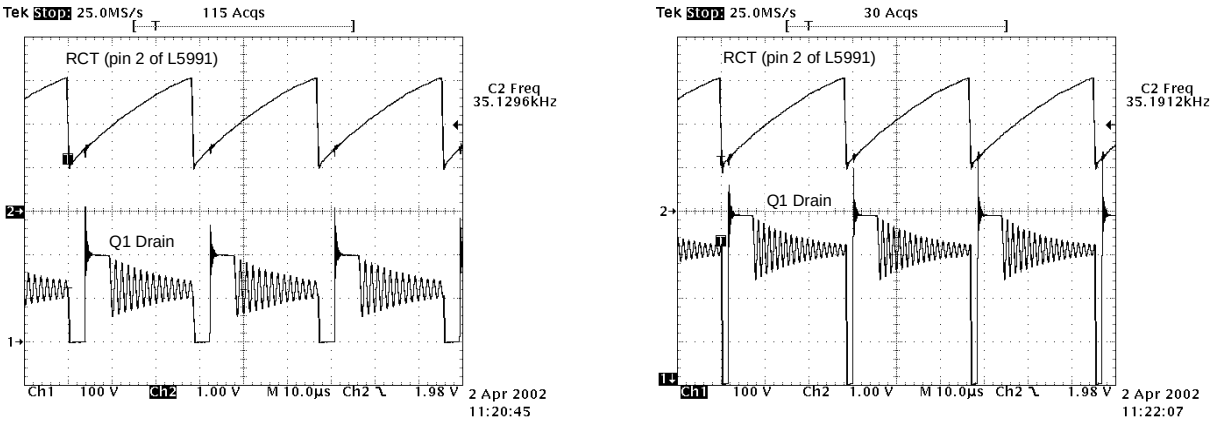
Figure 6. 45W AC-DC adapter: waveforms @ P_{out} = 45W



Vin = 110 Vac, Pout = 45W

Vin = 220 Vac, Pout = 45W

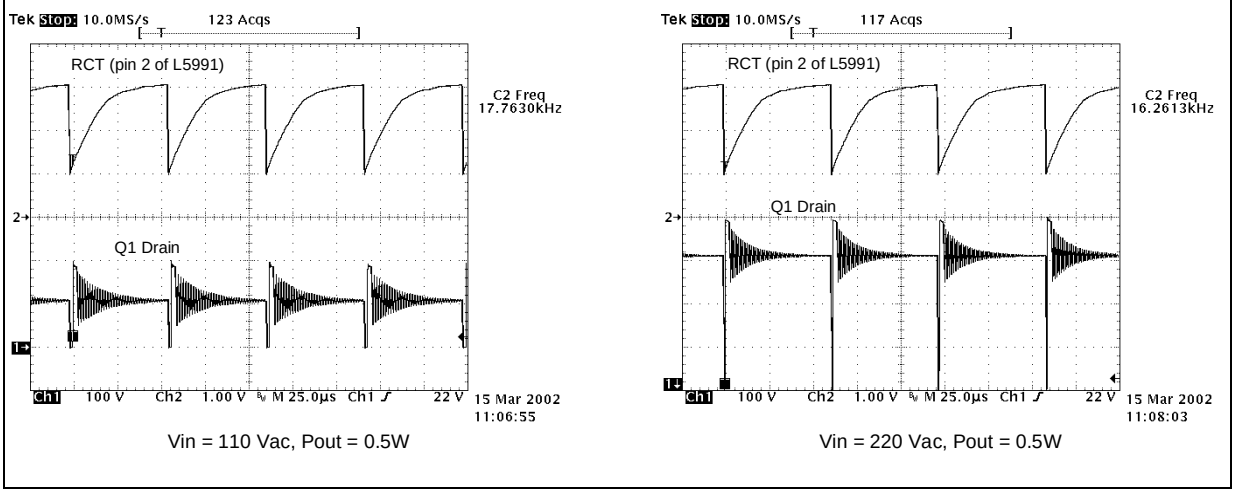
Figure 7. 45W AC-DC adapter: waveforms @ P_{out} = 7W, just after the abrupt frequency shift



Vin = 110 Vac, Pout = 7W

Vin = 220 Vac, Pout = 7W

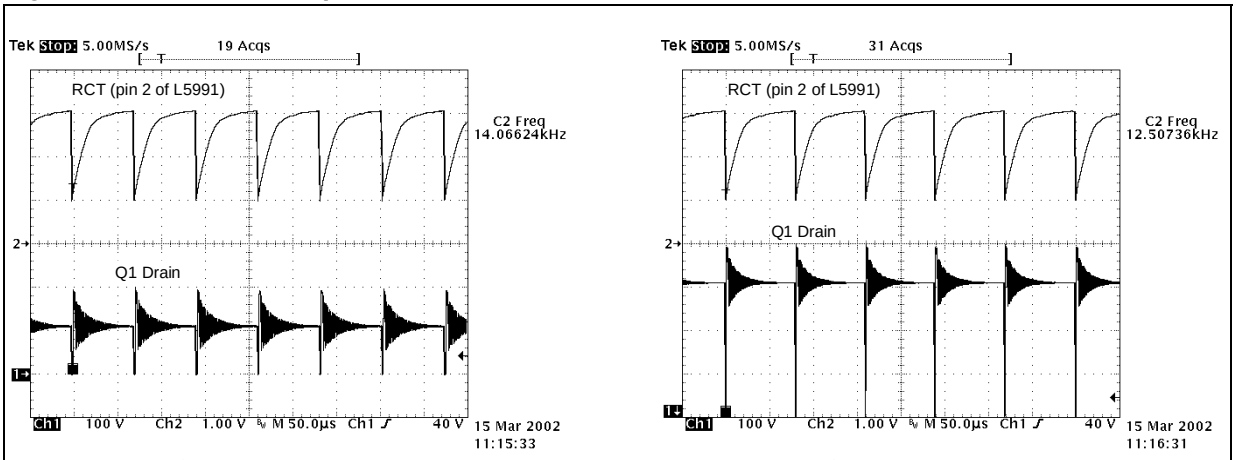
Figure 8. 45W AC-DC adapter: waveforms @ P_{out} = 0.5W



Vin = 110 Vac, Pout = 0.5W

Vin = 220 Vac, Pout = 0.5W

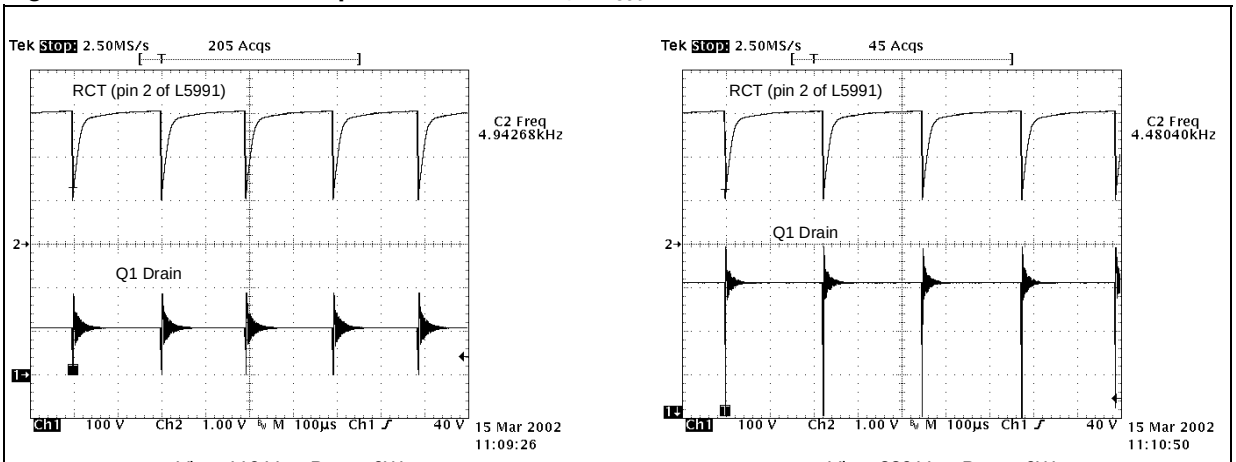
Figure 9. 45W AC-DC adapter: waveforms @ P_{out} = 0.3W



Vin = 110 Vac, Pout = 0.3W

Vin = 220 Vac, Pout = 0.3W

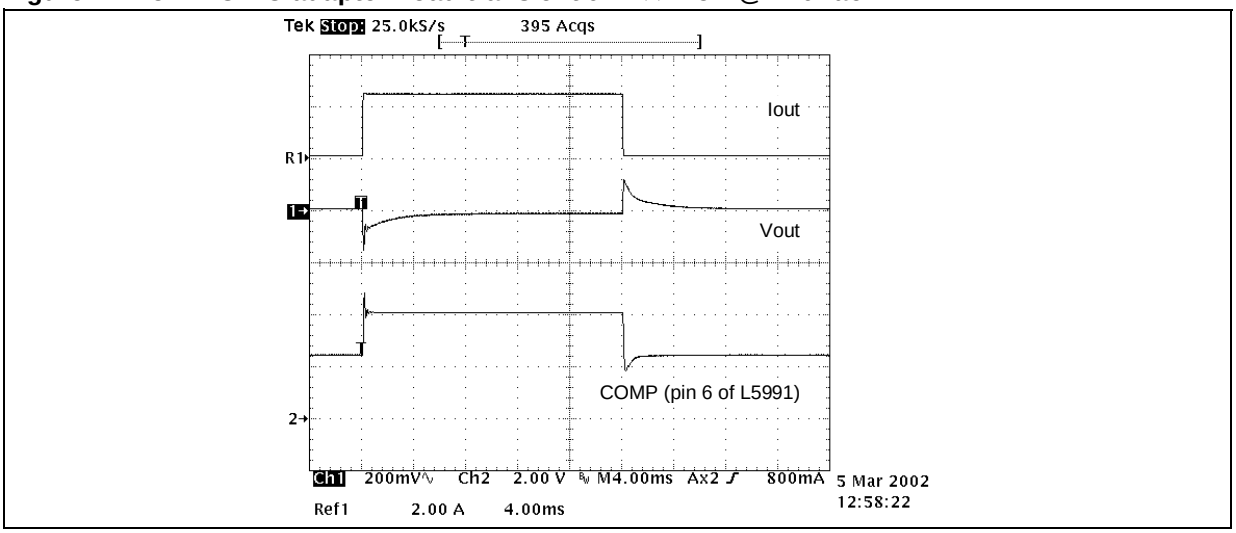
Figure 10. 45W AC-DC adapter: waveforms @ P_{out} = 0W



Vin = 110 Vac, Pout = 0W

Vin = 220 Vac, Pout = 0W

Figure 11. 45W AC-DC adapter: load transient 0.1 ⇔ 2.5A @ 220Vac



Optimization of a 80W AC-DC adapter with PFC

Table 4 summarizes the items of the electrical spec of this adapter more relevant to this context. Please refer to [4] for full electrical spec and evaluation data, as well as for a detailed description.

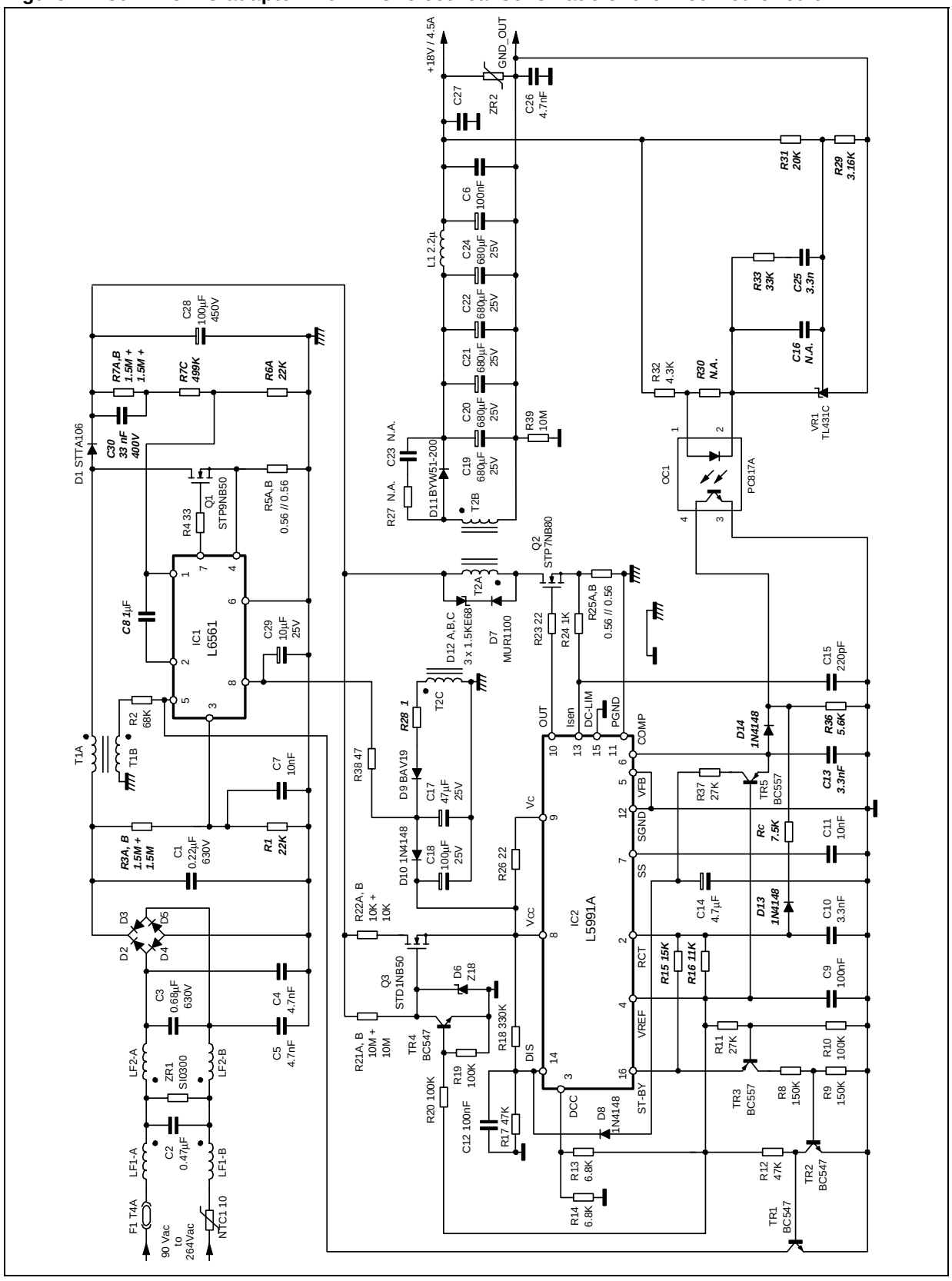
Table 4. 80W AC-DC adapter with PFC: electrical specification of the original design

Input Voltage Range (V_{in})	90 to 265Vac
Mains Frequency (f_L)	50/60Hz
Maximum Output Power (P_{outmax})	80W
Output	V_{out} = 18Vdc ± 2% I_{out} = 0 to 4.5A V_{ripple} ≤ 1%
Line and Load regulation	< 1%
Switching Frequency (Flyback, @ P_{out} = 80W)	65kHz
Switching Frequency (Flyback, @ P_{out} = 0W)	20kHz
Target Overall Efficiency (@ P_{out} = 80W, V_{in} = 90÷265Vac)	η > 75%
Maximum No-load Input Power (V_{in} = 90 ÷265Vac)	< 1W

The full-load input power is greater than 100W, then this adapter is actually out of the scope of the ECC. Its no load consumption (0.9W @265Vac, 0.7W @220 Vac), however, is within the Phase 1 limit (1W) and not far from that of Phase 2 and 3 (0.75W @230 Vac) for the highest power bracket.

Again, the target of the optimization is to meet Phase 3 limit @Vin = 264 Vac. Figure 12 shows the electrical schematic with the added and modified components highlighted. Only these changes, which track those made in the previously considered design plus those related to the PFC stage, will be discussed

Figure 12. 80W AC-DC adapter with PFC: electrical schematic of the modified circuit



1 The oscillator of the L5991 has been modified to maintain the same frequency under normal operation (65kHz) at full load and have a standby frequency of 36kHz. Also in this case the oscillator frequency with no-load is chosen 5kHz. Further details on the calculations can be found in the appendix.

2 Again, the dummy load represented by the feedback components on the secondary side has been reduced at about 40mW (see the same point of the previous design).

3 The frequency compensation of the voltage control loop (C7, C14, R20) has been modified so as to double the bandwidth and get a faster response (especially useful at start-up).

4 R28 has been decreased from 3.3 to 1Ω, to prevent the supply voltage of the L5991A from going below the UVLO threshold with no load, while not exceeding the rating of both the L5991A and the L6561.

5 The multiplier bias resistors (R3A = R3B = 680k Ω and R1 = 10 kΩ) of the L6561 consume 103mW @264 Vac, then their value has been more than doubled (R3A = R3B = 1.5M Ω and R1 = 22kΩ). In this way their maximum consumption is reduced at 46mW @264 Vac.

6 The output divider of the PFC pre-regulator (R7A = R7B = 499k Ω and R1 = 6.34kΩ) gives origin to a consumption of 140mW @264 Vac. With the aim of reducing the consumption at 40mW maximum, while not degrading the dynamic OVP function, the feedback network has been modified as shown in figure 13. The capacitor bypasses the two 1.5M Ω resistors during output voltage overshoots, resulting in a only slightly higher OVP threshold, as compared to the original one. The positive side-effect is an improvement of the transient response of the PFC pre-regulator. The components for the frequency compensation of the error amplifier of the L6561 have been changed consequently.

The modifications are summarized in table 5.

Figure 13. Modified PFC pre-regulator's feedback and frequency compensation network

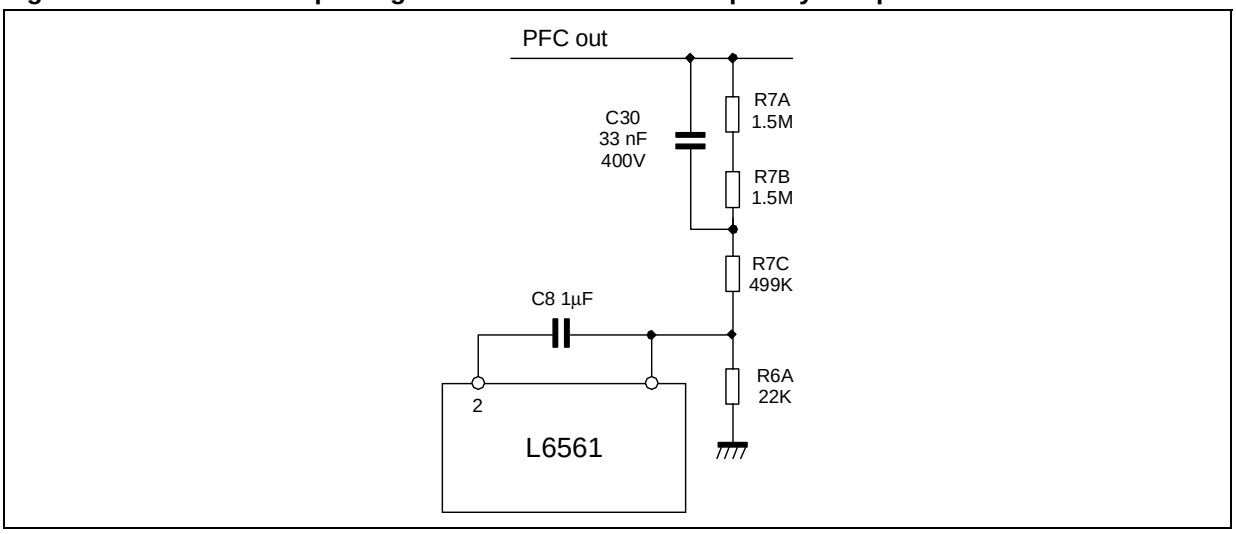


Table 5. 80W AC-DC adapter with PFC: list of modifications to the original design

Part	Original value	New Value	Part	Original value	New Value
R1	10kΩ	22kΩ	R31	2.2kΩ	20kΩ
R3A, R3B	680kΩ	1.5MΩ	R33	13kΩ	33kΩ
R6A	6.34kΩ	22kΩ	R34	510kΩ	---
R7A, R7B	499kΩ	1.5MΩ	R35	2.2kΩ	shorted
R7C	---	499kΩ	R36	10kΩ	5.6kΩ
R15	10kΩ	15kΩ	R_C	---	7.5kΩ
R16	22kΩ	11kΩ	C13	15nF	3.3nF
R28	3.3Ω	1Ω	C25	330nF	3.3nF
R29	348Ω	3.16kΩ	C30	---	33nF / 400V
R30	1.2kΩ	---	D13, D14	---	1N4148

80W AC-DC adapter with PFC: evaluation results

The following diagrams compare the performance of the original design ("standard standby") with that of the modified one ("improved standby").

To be noted in figure 14, the no-load consumption is slightly less than 0.5W @ 264Vac, then the modified 80W adapter now meets the ECC limits, Phase 3 for the 15-50W bracket (< 0.5W @230Vac).

Figure 14. 80W AC-DC adapter with PFC: light load input consumption comparison

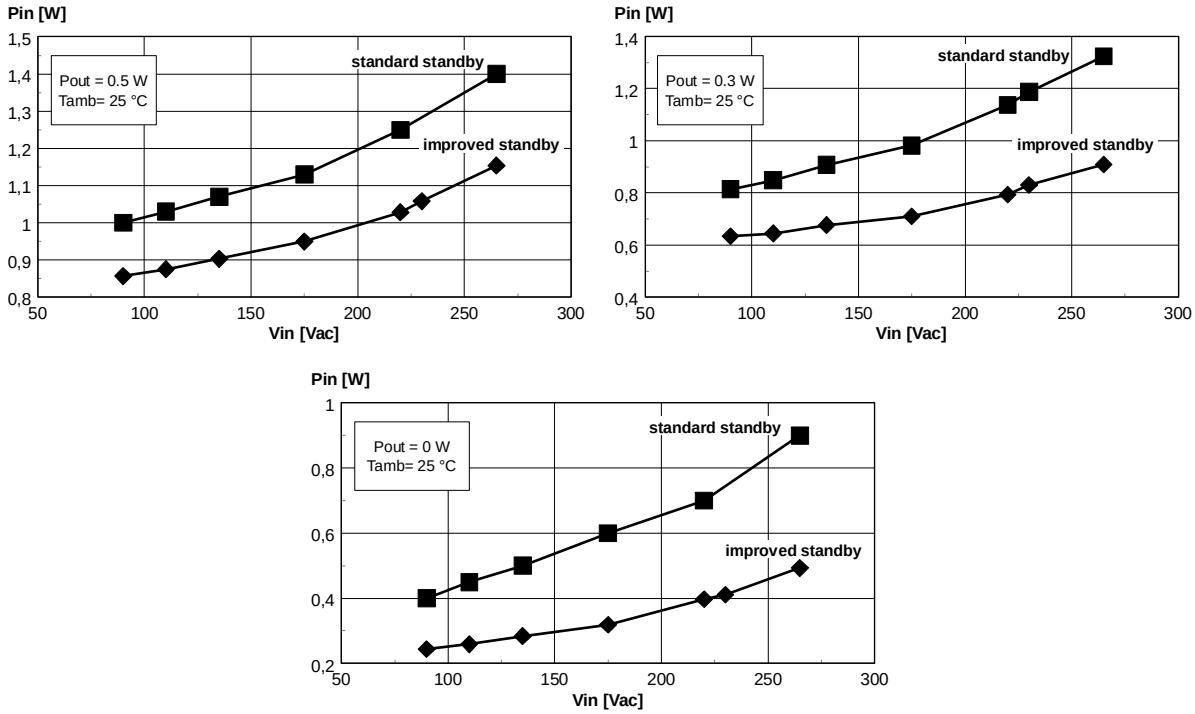


Figure 15. 80W AC-DC adapter with PFC: f_{sw} vs. I_{out} (left); f_{sw} vs. V_{in} (right)

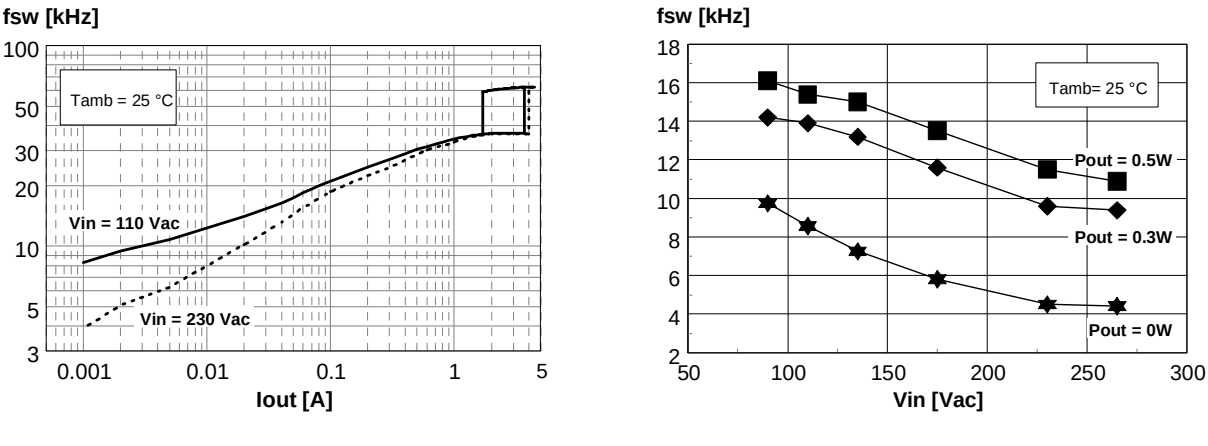
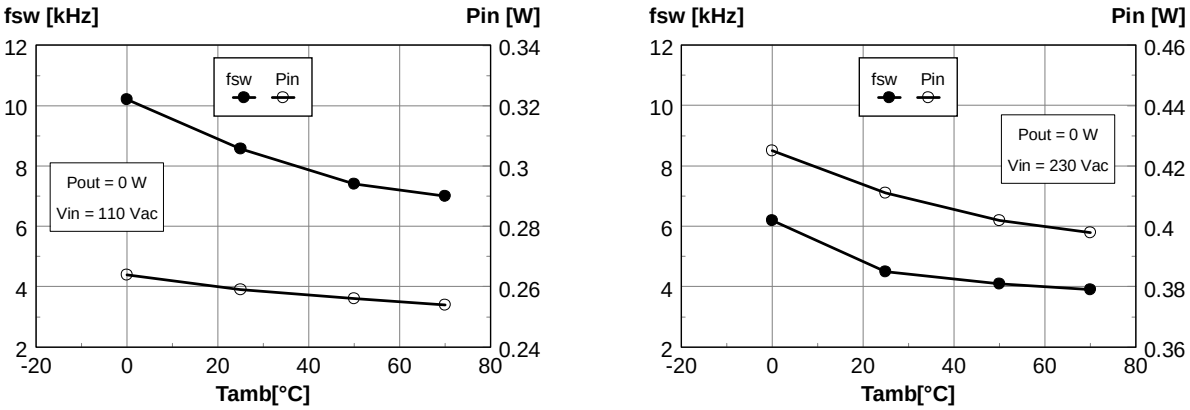


Figure 16. 80W AC-DC adapter with PFC: P_{in} (@ P_{out} = 0) and f_{sw} vs. ambient temperature



The diagrams in figure 15 illustrate the relationship between output current, input voltage and switching frequency obtained with the modified oscillator. Unlike the previously considered design, in this case the internal propagation delay of the current sense pin is not compensated, then V_{COMP} changes slightly with the input voltage and then there is a variation of the oscillator frequency.

The diagrams of figure 16 illustrate the very limited temperature effect on both the oscillator frequency and the no-load input consumption at both nominal voltages in the temperature range 0-70 °C.

Figure 17. 80W AC-DC adapter with PFC, flyback section: waveforms @ P_{out} = 80W

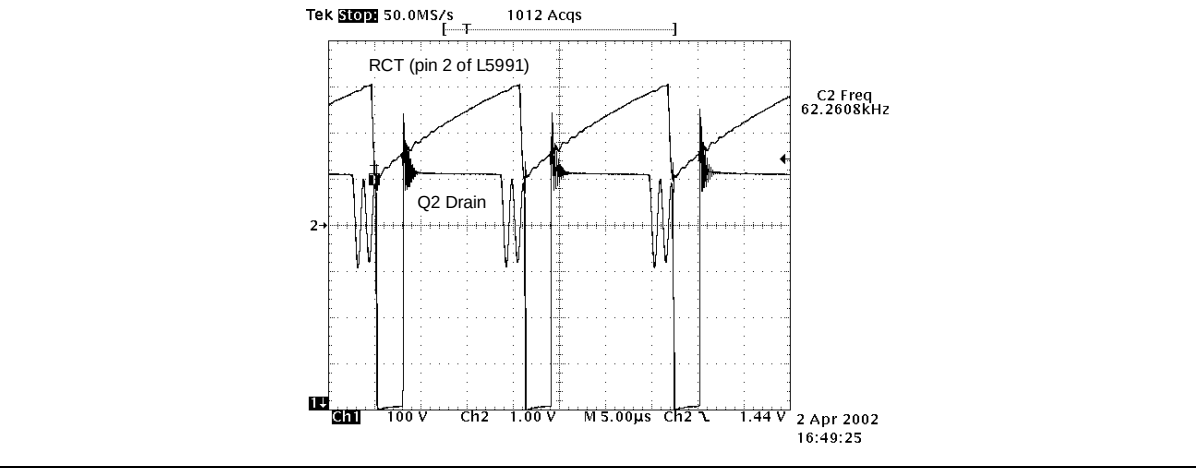


Figure 18. 80W AC-DC adapter with PFC, flyback section: waveforms @ P_{out} = 30W

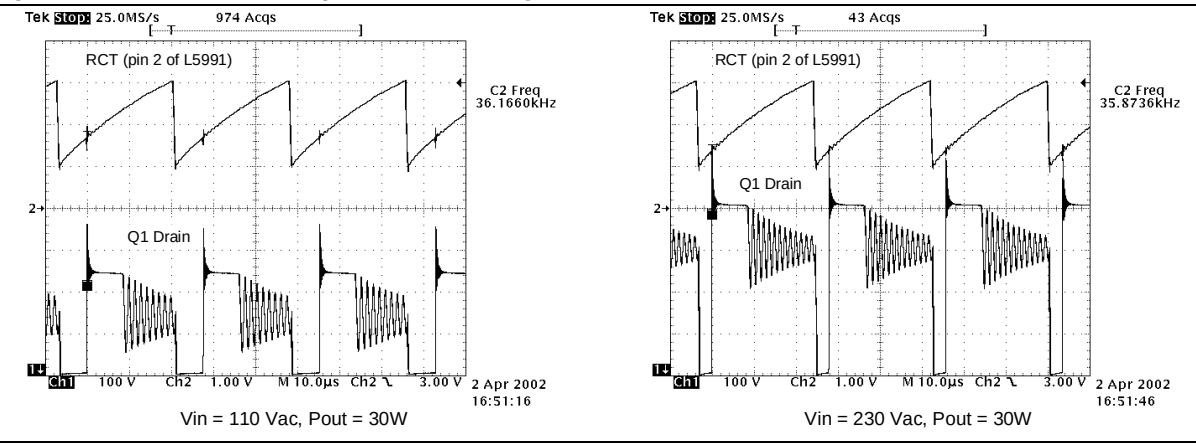


Figure 19. 80W AC-DC adapter with PFC, flyback section: waveforms @ P_{out} = 0.5W

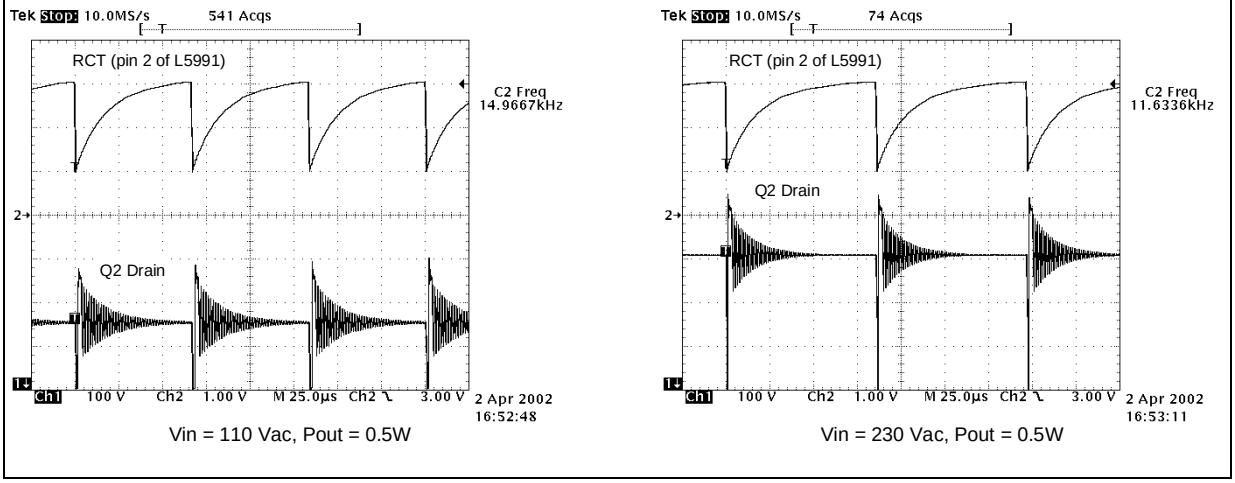


Figure 20. 80W AC-DC adapter with PFC, flyback section: waveforms @ P_{out} = 0.3W

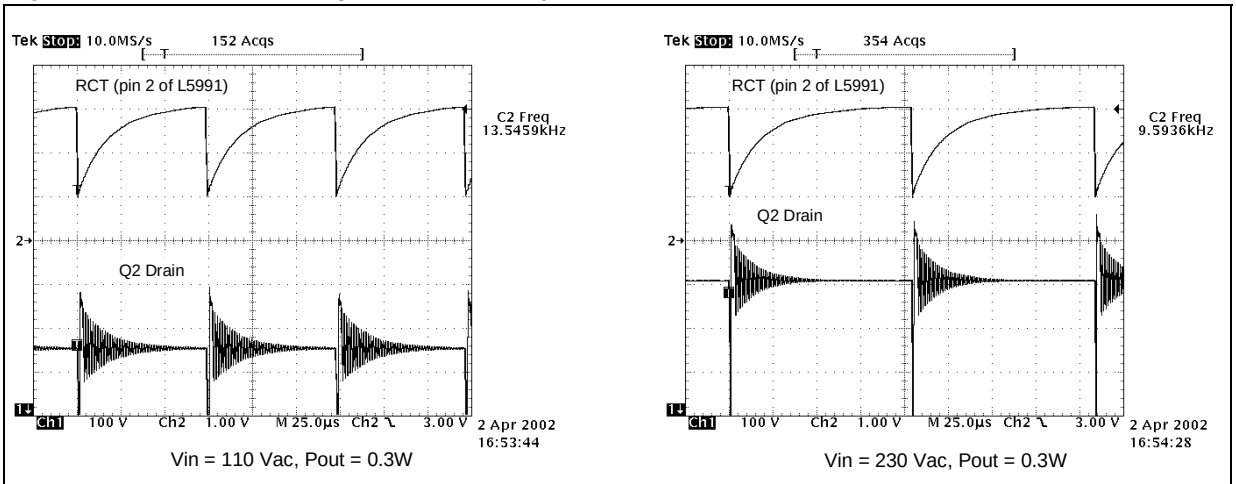


Figure 21. 80W AC-DC adapter with PFC, flyback section: waveforms @ P_{out} = 0W

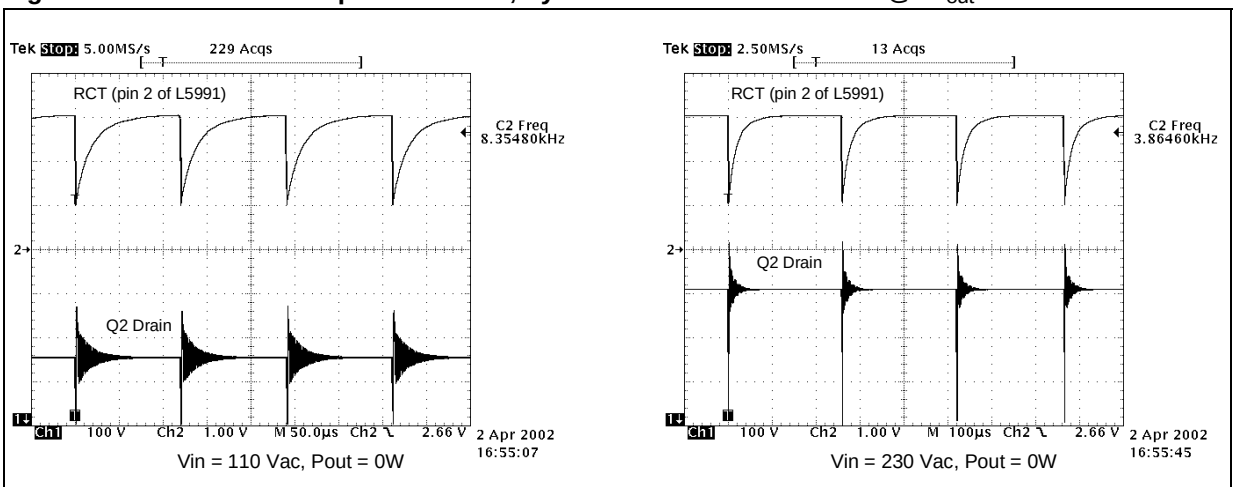
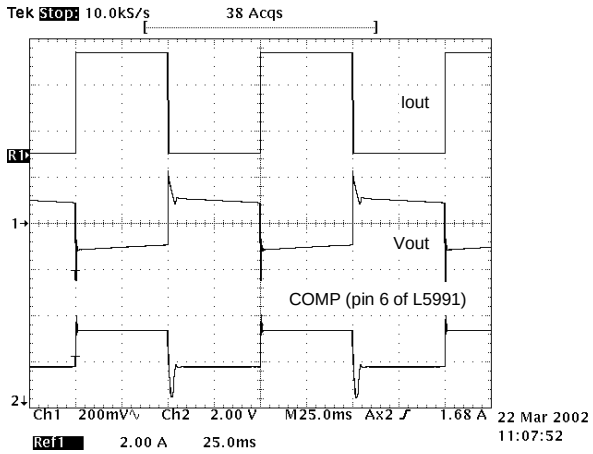


Figure 22. 80W AC-DC adapter with PFC, flyback section: load transient 0.1 ⇔ 4.5A @ 220Vac



Conclusions

A simple modification of the oscillator allows optimizing L5991-based converters to achieve a considerable decrease of the no-load consumption. This has been proved in a 45W AC-DC adapter and in an 80W power-factor-corrected adapter, where the optimization here proposed has brought a reduction of the no-load input consumption up to 400mW at high line.

This is the result of concurrent improvements. The modification to the oscillator allows very low switching frequency under no-load conditions without a large f_{osc} to f_{SB} ratio. The resulting lower V_{COMP} jump provides more headroom for overshoots and undershoots, so that it has been possible to enlarge the bandwidth of the control loop without any frequency instability. In turn, the faster response due to the larger bandwidth has allowed the reduction of the dummy load on the output, without compromising correct start-up when the adapter is unloaded. The lower residual load and the loss reduction due to the very low oscillator frequency, results in a dramatic decrease of the power absorbed from the mains at no load.

REFERENCES

[1] "L5991/L5991A Primary Controller with Standby" Datasheet
[2] "Minimize Power Losses of Lightly Loaded Flyback Converters with the L5991 PWM Controller" (AN1049)
[3] "45W AC-DC Adapter with Standby Function" (AN1134)
[4] "80W Power-factor-corrected AC-DC Adapter with Standby Using the L6561 and the L5991A" (AN1440)

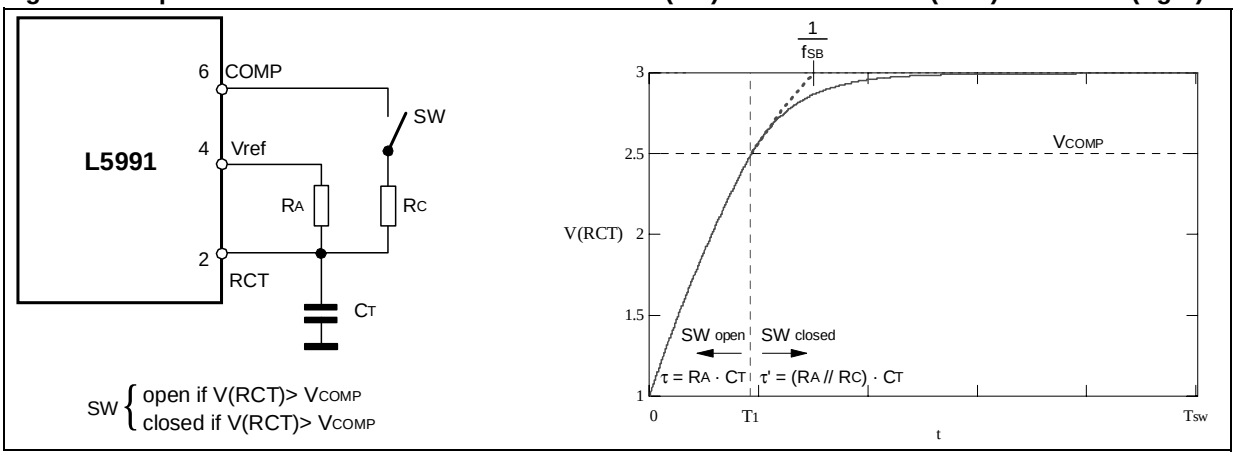
APPENDIX

How to calculate R_C and R'.

As previously said in the section *"Standby function improvement"*, there is no change for the calculation of the timing components C_T, R_A, R_B because R_C is disconnected by the series diode D1 when V_{COMP} > 3V. Then only the calculation of R_C to get a given f_{min}, as well as that of R' needs to be taken into consideration.

To this end it is necessary to consider first the timing equations that govern the operation of the oscillator. Refer to figure A1 for the equivalent circuit and the relevant waveform, which assume that D1 and D2 match.

Figure A1. Equivalent circuit for oscillator calculations (left) and theoretical V(RCT) waveform (right)



As long as the oscillator voltage V(RCT) is less then V_{COMP}, D1 is reverse-biased (SW is open) and only R_A contributes to the time constant τ; moreover, the asymptote of the exponential curve is the reference voltage V_{REF} (5V). When V(RCT) equals and exceeds V_{COMP}, D1 is forward-biased (SW is closed), then R_C goes in parallel to R_A to determine the time constant τ' and the asymptote will be changed to:

$$V_{REF}\frac{R_C}{R_A + R_C} + V_{COMP}\frac{R_A}{R_A + R_C} < V_{REF}$$

Note that the new time constant τ' is shorter, then it will be the lower asymptote the responsible for getting a longer oscillator period. The complete equation describing the oscillator is then

$$V(RCT) = \begin{cases} V_V + (V_{REF} - V_V)\left(1 - e^{-\frac{t}{\tau}}\right) & t \le T_1 \\ V_{REF}\frac{R_C}{R_A + R_C} + V_{COMP}\frac{R_A}{R_A + R_C} - \frac{R_C}{R_A + R_C}(V_{REF} - V_{COMP})e^{-\frac{t - T_1}{\tau'}} & t > T_1 \end{cases} \quad \text{(A1)}$$

where:

$$T_1 = \tau \ln\frac{V_{REF} - V_V}{V_{REF} - V_{COMP}} = \tau \ln\frac{4}{5 - V_{COMP}}$$

is the time when V(RCT) = V_{COMP} and R_C comes into play (i.e. SW is closed), V_V is the oscillator valley voltage (1V) and the time constants τ and τ' are defined as shown in figure A1.

To find a simple formula to calculate R_C some simplifications are necessary. Usually $T_1 << T_{sw} = 1/f_{min}$, then T_1 will be neglected and it is possible to write:

$$V_{pk} = V_{REF}\frac{R_C}{R_A + R_C} + V_{COMP_0}\frac{R_A}{R_A + R_C} - \frac{R_C}{R_A + R_C}(V_{REF} - V_{COMP_0})e^{-\frac{T_{SW}}{\tau'}}, \quad \text{(A2)}$$

where V_{pk} is the oscillator peak voltage (3V) and V_{COMP0} the value of V_{COMP} under no-load conditions. But, if $T_1 << T_{sw}$ it will be also $\tau' << T_{sw}$ and the exponential term in (A2) can be neglected. Then (A2) becomes:

$$V_{pk} = V_{REF}\frac{R_C}{R_A + R_C} + V_{COMP_0}\frac{R_A}{R_A + R_C}$$

that, solved for R_C, yields:

$$R_C = R_A\frac{V_{pk} - V_{COMP_0}}{V_{REF} - V_{pk}} = R_A\frac{3 - V_{COMP_0}}{2} \quad . \quad (A3)$$

The maximum value for R' can be calculated by imposing that D2 be always forward-biased, that is its current never fall to zero, with $V_{COMP} = V_{COMP0}$. The current flowing through D2 is:

$$I_{D2} = \frac{V_{COMP_0} - V_F}{R'} - I_{D1} \ ,$$

while the maximum current flowing through D1 is:

$$I_{D1x} = \frac{V_{pk} - V_F - (V_{COMP_0} - V_F)}{R_C} = \frac{V_{pk} - V_{COMP_0}}{R_C} = \frac{3 - V_{COMP_0}}{R_C} \ .$$

Then, imposing $I_{D2} > 0$ with $I_{D1} = I_{D1x}$ and solving for R', it is possible to obtain:

$$R' < R_C\frac{V_{COMP_0} - V_F}{V_{pk} - V_{COMP_0}} = R_C\frac{V_{COMP_0} - V_F}{3 - V_{COMP_0}} \quad . \quad (A4)$$

Since I_{D1} and I_{D2} are typically in the hundred µA, with good approximation it is possible to assume V_F = 0.5V @ 25°C in (A4). Worst-case scenario is at minimum operating temperature: -2.5 mV/°C drift can be considered to take this into account.

The point is now to calculate the value of V_{COMP0}. In [2] it is shown that in L5991-based flyback converters the following relationships holds true:

$$V_{COMP} = 1.4 + 3\left[Rs\left(\sqrt{\frac{2P_{in}}{f_{sw}L_p}} - \frac{V_{in}}{L_p}T_{delay}\right) + V_o\right] \ , \quad (A5)$$

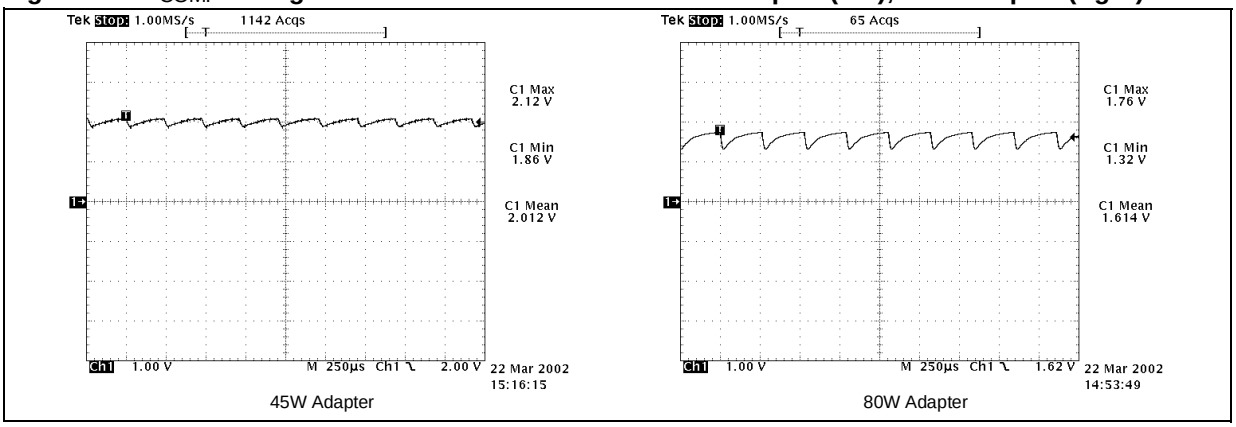
where Rs is the sense resistor (R15 in figure 3, R25 in figure 12), P_{in} the input power to the transformer, L_p its primary inductance, V_{in} the DC input voltage to the converter, T_{delay} the internal propagation delay of the current sense pin (200 ns typ.) and V_o a DC voltage offset that can be applied to the current sense pin.

In case the offset V_o is chosen equal to

$$Rs\frac{V_{in}}{L_p}T_{delay} \ ,$$

the effect of the propagation delay is compensated and V_{COMP} will no longer depend on the input voltage V_{in}. That is the case of the 45W adapter, where the job is done by R3 and R4 along with R14. For the 80W adapter there is no compensation (V_o = 0) then there will be a slight dependence of V_{COMP} (and then of the oscillator frequency when R_C is active) on V_{in}. This is confirmed by the experimental results.

Figure A2. V_{COMP} **voltage under no-load conditions: 45W adapter (left), 80W adapter (right)**



To calculate V_{COMP0}, P_{in} needs to be estimated considering the power processed by the transformer under no-load conditions. It is possible to use the following formula:

$$P_{in} = 1.25(V_{out}\, I_{outres} + V_{aux}\, I_{aux}) , \quad (A6)$$

where I_{outres} is the residual output current (through the output divider, through the optocoupler's LED, as well as any residual dummy load resistor), V_{aux} is the voltage generated by the auxiliary winding that supplies the L5991 (and the L6561 in the 80W adapter) and I_{aux} the total consumption on this winding (quiescent current of the L5991, of the L6561 too in the 80W adapter, optocoupler's transistor current and the consumption of any circuit supplied by the reference voltage of the L5991 or directly connected to its supply bus). The coefficient 1.25 stems from an estimated efficiency of 80% that experiments have shown many flyback transformers feature under no-load conditions, almost regardless of their size, parameters and construction.

It is obvious that the estimate of P_{in} is the weak point of this design procedure. Since it is essentially the asymptote of the oscillator waveform that governs the oscillator frequency, even some ten mV variation of V_{COMP0} may change the frequency considerably. A small error in the assessment of V_{COMP0}, then, could lead to a value for R_C that gives an f_{min} away from the target. This is why it is recommended to use the result of the calculation as a starting point that has to be checked on the bench and, in case, corrected after the experiments. For completeness, it must be said also that under no-load conditions V_{COMP} is far from being a perfect DC voltage, as shown in the diagrams of figure A2.

45W adapter example calculation

With C_T = 3.3nF, R_A and R_B are 12kΩ each. The residual output load is 40mW, the total consumption of the auxiliary winding is estimated around I_{aux} = 10mA, that is 110mW assuming V_{aux} = 11V. Then, using (A6):

$$P_{in} \approx 1.25\ (0.04 + 0.11) = 0.188W .$$

V_{COMP0} will be given by (A5), where it is assumed a perfect propagation delay compensation:

$$V_{COMP_0} = 1.4 + 3 \cdot 0.47 \sqrt{\frac{2 \cdot 0.188}{5 \cdot 10^3 \cdot 400 \cdot 10^{-6}}} = 2.011V .$$

From (A3):

$$R_C = 12 \cdot 10^3 \frac{3 - 2.011}{2} = 5.934 \cdot 10^3 \quad \text{use standard value 5.9k}\Omega.$$

From (A4), considering T_{amb} = 0°C, then V_F = 0.563V:

$$R' < 5.9 \cdot 10^3 \frac{2.011 - 0.563}{3 - 2.011} = 8.638 \cdot 10^3 \quad \text{use standard value 8.2k}\Omega.$$

80W adapter example calculation

With C_T = 3.3nF, we get R_A =15kΩ and R_B = 11kΩ. The residual output load is 40mW, the total estimated consumption of the auxiliary winding is I_{aux} = 12mA, that is 120mW assuming V_{aux} = 10V. Then, using (A6):

$$P_{in} \approx 1.25\ (0.04 + 012) = 0.2W$$

V_{COMP0} will be given by (A5):

$$V_{COMP_0} = 1.4 + 3 \cdot 0.28\left(\sqrt{\frac{2 \cdot 0.2}{5 \cdot 10^3 \cdot 430 \cdot 10^{-6}}} - \frac{375 \cdot 200 \cdot 10^{-9}}{430 \cdot 10^{-6}}\right) = 1.616V .$$

From (A3):

$$R_C = 11 \cdot 10^3 \frac{3 - 1.616}{2} = 7.612 \cdot 10^3 \quad \text{use standard value 7.5k}\Omega$$

From (A4)), considering T_{amb} = 0 °C, then V_F = 0.563 V:

$$R' < 7.5 \cdot 10^3 \cdot \frac{1.616 - 0.563}{3 - 1.616} = 5.706 \cdot 10^3 \quad \text{use standard value 5.6k}\Omega.$$