A logic-level transient-voltage protected AC switch

Introduction

Home appliances such as washing machines, refrigerators, and dishwashers employ a lot of low power loads such as valves, door lock systems, dispensers, or drain pumps. Since these loads are powered by the mains in ON/OFF mode, they were initially controlled by relays. Today, relays have been replaced by triacs, due to their smaller size and lower driving energy. Nevertheless, triacs do not alone fulfill the new requirements that users now need and are used with other components.

Power switches must now be directly driven by a microcontroller unit (MCU) and must be robust to withstand the A.C. line transients so that systems may fall into line with electromagnetic compatibility (EMC) standards. ACSs (for alternating current switches) have been designed with this goal in mind, that is, to offer logic level and more robust semiconductor devices.

On the other hand, ACSs have been developed adopting a functional integration approach. They can be used directly between an MCU and the load. An external protection, or a buffer circuit is not required since these are already integrated on the die. This considerably reduces the overall electronic board size.

Table 1 gives the typical RMS current of loads that can be controlled by ACS108-8SA, in ON/OFF control mode.

Table 1. ACS108 targeted loads

Load	I_{RMS} (A)	Power factor	$(dI_{out}/dt)c$ (A/ms)	$(dV_{out}/dt)c$ (V/µs)	Turn-off delay (ms)
Door lock	< 0.3	1	0.15	0.15	< 10
Lamp	< 0.8	1	0.4	0.15	< 20
Relay, valve, dispenser, micromotor	< 0.1	> 0.7	< 0.05	< 2	< 10
Pump	< 0.2	> 0.2	< 0.1	< 10	< 10
Fan	< 0.6	> 0.2	< 0.3	< 10	< 20

1 ACS triggering mode

1.1 Negative gate current

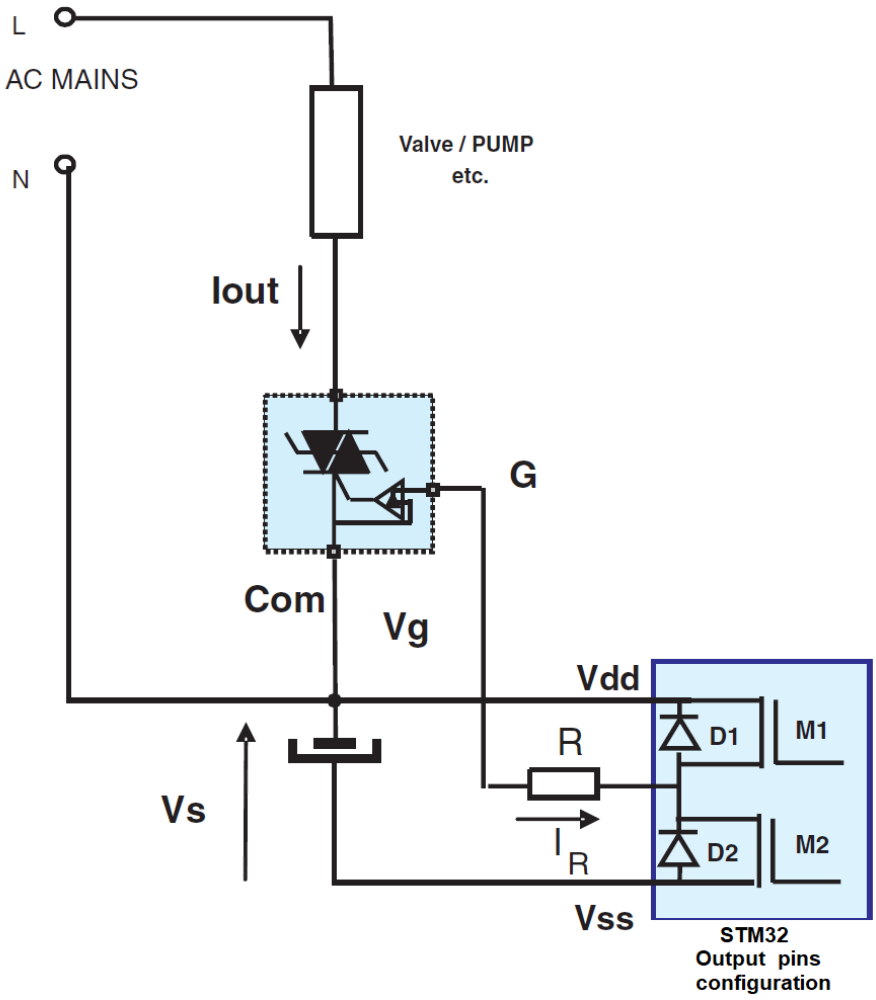
The ACS silicon structure is different from the triac one. For instance, the gate embeds a diode junction. Then the gate current can only circulate in one direction, from the COM pin to the gate one. A peak reverse voltage (V_{GM}) of this junction is also defined in the ACS datasheet.

To sink a current from the gate by a microcontroller output port, the supply voltage positive terminal must be connected to the drive reference, that is, the COM pin of ACSs (see Figure 1).

An interesting benefit of such a connection is that the ACS is not fired when the MCU is at reset state. Indeed, in this case, all the MCU port pins are at high level. This means that the gate resistors are all connected to the COM terminal. No spurious triggering can then occur.

It should be noticed that for a direct switch / MCU connection, the MCU current capability is not the only point to check to decide if the buffer circuit can be removed. Actually, the transistor, used to amplify the MCU current to control the gate, also play an overvoltage protection role. Section Appendix D gives the gate voltage limits between which the MCU output port is not stressed. It is also shown that with ACSs, the gate voltage remains inside these limits even with worst cases of dI/dt gradients at turn-on.

Figure 1. Gate / MCU connection

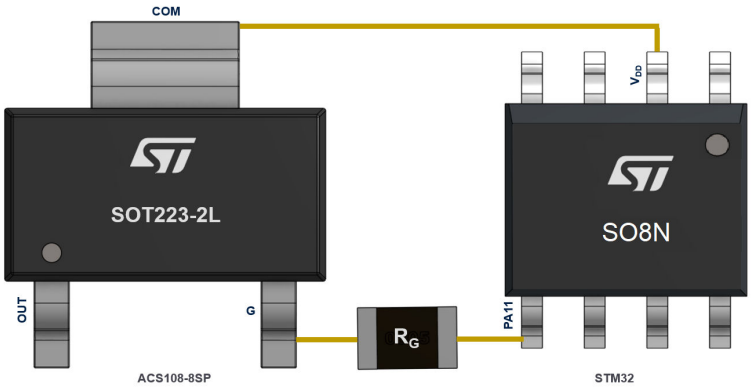


1.2 New layout possibilities

It has already been said that the ACS silicon structure is different from the triac, according to the gate operation. A second difference is that the ACS have been developed in an integration goal.

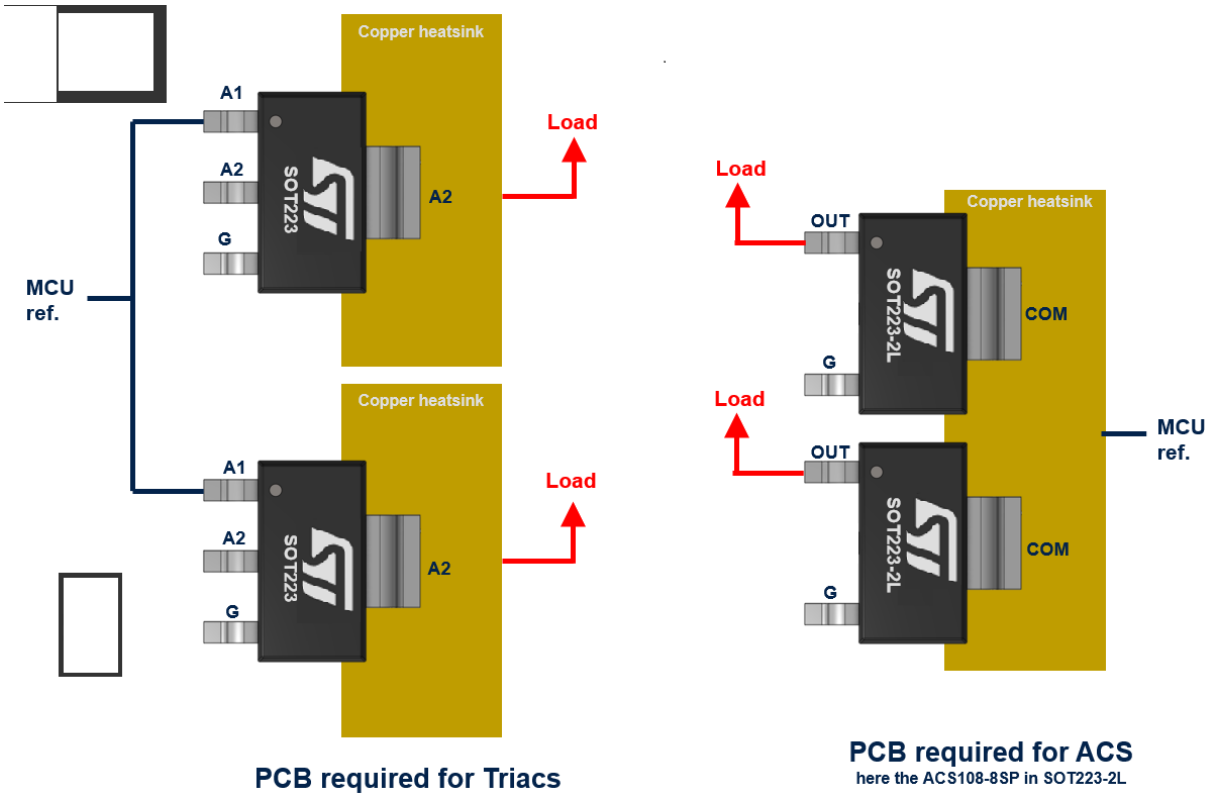
To allow different cells to be associated in one single package or controlled by one single drive die, the common drive reference voltage must be connected to the back of the die. Indeed, each die bottom is electrically linked to the other ones by the frame. This is achieved by the ACS silicon structure, where an integrated level shifter allows both thyristors to be controlled by means of a gate voltage referenced at the back of the die (COM pin). (See [1]).

Figure 2. STM32 to ACS108: the easy connection



A particular benefit of such a pin out appears with surface mount devices (SMD). In this case, the tab pin is the COM. The copper surface used to perform a heat-sink can then be used as a supply voltage bus. It offers new layout possibilities and, above all, a miniaturization of the printed circuit board (PCB). Indeed, unlike triacs, the heat-sink areas are at the same voltage and so can be regrouped (see Figure 3). The heatsink area therefore depends on the maximum amount of dissipated power at the same time, by all the switches put on it. So, the number of switches, which conduct at the same time and their conduction time should be known.

Figure 3. Printed circuit area reduction thanks to ACSs in SOT223 packages

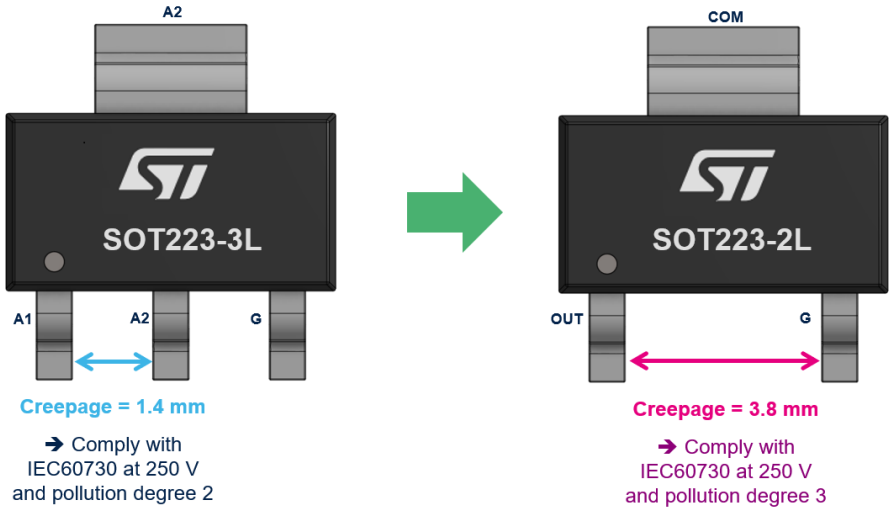


1.3 ACS108-8SP

The ACS108-8SP introduces the augmented SOT223-2L package. This high creepage SMD is tolerant for high pollution degree meaning that electronics designers have no more to encapsulate SOT223 pins into potting to withstand functional application voltage in a polluted or wet environment.

As described in the figure below, the standard SOT223-3L creepage is 1.4 mm and offer withstand 250 V with pollution degree 2, the SOT223-2L is compliant with the IEC60730 standard with pollution degree 3 while keeping the SOT223 like package other performances.

Figure 4. Standard SOT223-3L creepage



The pollution degree definition given by IEC60730 is the following:

- Pollution degree 2: Only non-conductive pollution occurs, except that occasionally a temporary conductivity caused by condensation is to be expected.
- Pollution degree 3: Conductive pollution occurs, or dry non-conductive pollution occurs that becomes conductive due to condensation that is to be expected.

2 Inductive loads on/off control

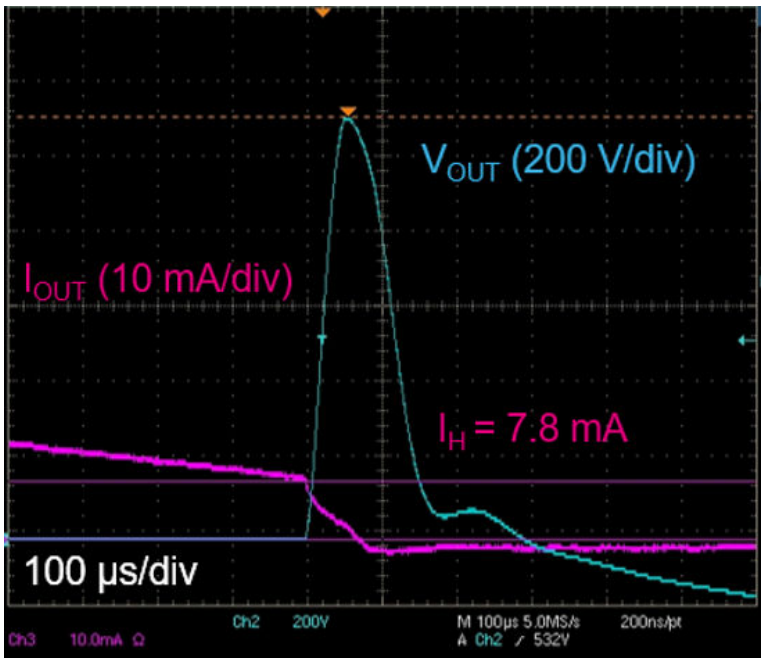
2.1 Valves and relays

2.1.1 Turn-off overvoltages are clamped by ACSs

Valves and relays are both electromagnetic systems. In the case of AC high voltage operation, their windings present a high series resistance (a few kΩ) and a high series inductance (tens of Henry). Hence, they absorb a low RMS current (typically, 10 to 50 mA). In this case, the current rate of decrease is low and an automatic switch turn-off may result, when its current becomes lower than the holding level (see [2]). There may be an overvoltage because there is still some current through the inductive load. The inductive energy thus creates a back electromotive voltage, which tends to force the switch to conduct. If this overvoltage is not clamped, it can exceed the device breakdown level and damage it.

ACSs are overvoltage self-protected. They can sustain their holding current in such an operating mode, as shown in Figure 5.

Figure 5. ACS voltage and current waveforms at turn-off (230 V 35 mA RMS valve)



During clamping periods, the inductive energy is dissipated both in the silicon die and the series resistance of the load. The worst case appears when the load inductance is the highest, that is, for electromagnet loads. In Section Appendix D a theoretical analysis is performed with a 0.1 power factor load and an RMS current lower than 40 mA (a value, which never appears in practice where, for such RMS currents, the power factor is always higher than 0.7). Then, it is demonstrated that, even in this worst case scenario, the transient junction temperature remains below 160 °C. And the clamping period time (t_{cl}) always lasts less than 1 ms. Such a thermal stress is suitable for ACSs dies thanks to their reliable planar technology.

2.1.2 Maximum switching frequency

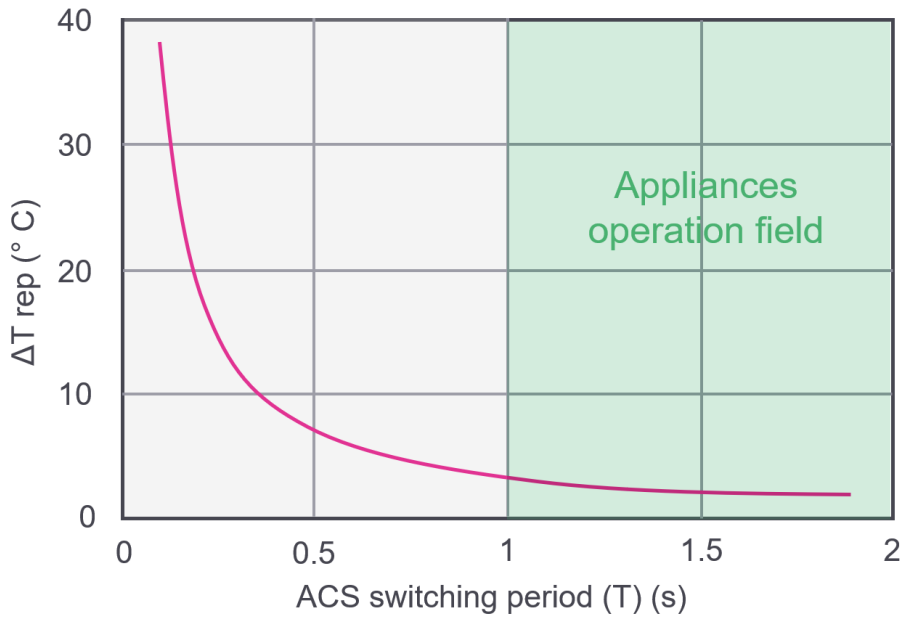
As far as thermal management involving clamping phases are concerned, a maximum load commutation frequency must be defined to avoid excessive device heating. Figure 6 gives the maximum supplementary temperature rise due to recurrent clampings, versus the ACS switching period (see Section Appendix D). This value is given for a 230 V - 50 Hz mains voltage (110 V mains is less stressing), for the worst case of load (power factor = 0.1, peak load current = i_H max) and for the maximum V_{CL} and i_H values (800 V and 60 mA respectively). In this case, the energy absorbed by the die equals 25 mJ.

The chosen package is the TO-92 one because it presents the highest R_{th} value, among the ACS packages on offer (TO-92, SO-8, SOT223, SOT223-2, DPAK).

It can be seen that this temperature elevation can be neglected (< 4°C) as long as the control frequency is less than one hertz. Such a value is suitable for most appliance applications where loads are at most controlled once per second. For that reason, in ACS datasheets, the maximum allowed current is given for a 1 hertz maximum frequency 0.1 minimum load power factor. Turn-off dissipated power is then reviewed for a wide range of application needs.

This enables us to conclude that no varistor is needed across ACSs to clamp the loads of inductive energy at turn-off, even with electromagnets, which are the highest inductive loads in appliances.

Figure 6. Supplementary temperature elevation due to repetitive clampings (at clamping energy = 25 mJ, package: TO-92)



2.2 Pumps and Fans ON / OFF control

2.2.1 Application requirements for (dI/dt)c and (dV/dt)c

There is a higher risk that a triac or an ACS fail to turn-off when both the load current rate of decrease and the reapplied voltage rate across the device are steep (see [3]). This risk increases as the junction temperature increases. The maximum current decreasing rate that ACS can switch off, called (dI/dt)c is defined for a maximum reapplied voltage rate, called (dV/dt)c, and for its maximum T_j.

Pumps and fans are, for the most part, induction or permanent magnet motors. Their series inductance is in the range of one Henry, and their winding resistance equals a few hundred ohms. Their power factor is low. Hence, after switch turn-off, the reapplied voltage across it is high and appears with a high rate of increase (as described in Eq. (1) where L and cosφ are the inductance and power factor of the load, V the mains RMS voltage and C is the ACS capacitance value).

$$\left(dV/\,dt\right)c_{(V/\mu s)} \cong V_{(V)}\sqrt{2}\sin(\varphi)\frac{10^{-8}}{\sqrt{L_{(H)}C_{(F)}}} \quad (1)$$

Figure 7 shows that the (dV/dt)c rate for an ACS108-8 die without snubber, controlling a 230 V 220 mA pump, is lower than 10 V/µs.

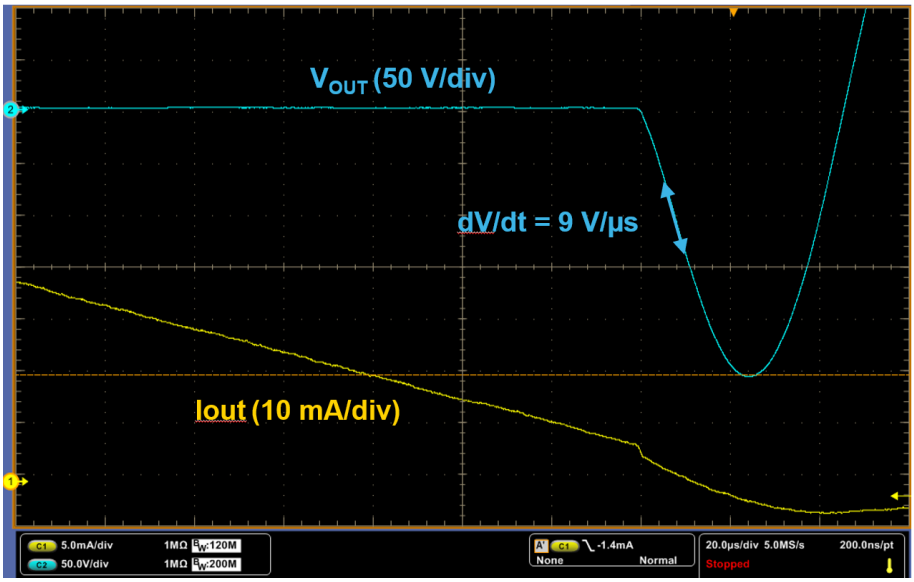
Eq. (2) shows that the current rate of decrease is almost half the RMS current (0.44 ratio for a 50 Hz mains frequency and 0.53 for 60 Hz).

$$(dI/dt)c_{(A/ms)} \cong \sqrt{2}I_{RMS(A)}2\pi f_{(Hz)}10^{-3} \quad (2)$$

To summarize, it can be said that the worst case commutation appears with pumps or fans. In this case, the stress that ACSs must withstand is:

$$(dI/dt)c_{(A/ms)} \cong 0.5I_{RMS(A)}; \left(dV/dt\right)c \leq 10V/\mu s \quad (3)$$

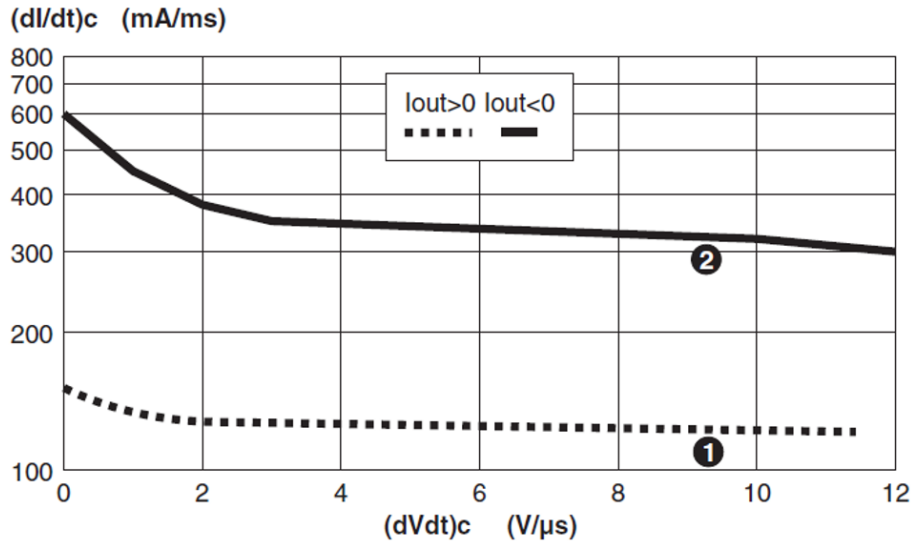
Figure 7. 230 V 220 mA RMS pump switch-off



2.2.2 ACS asymmetrical turn-off behavior

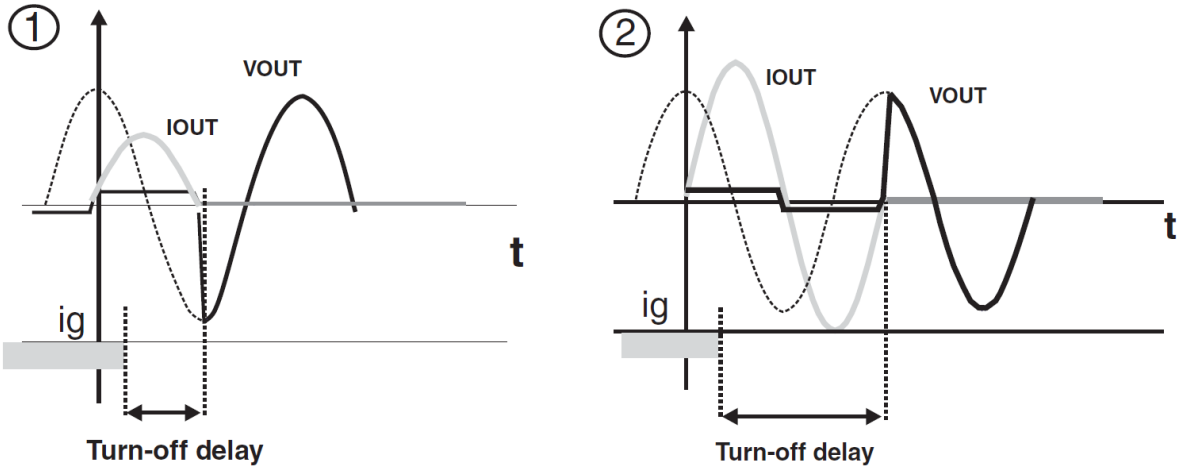
As shown in Figure 8, ACS108-8 behaves differently depending on the current direction before switch-off. This asymmetrical behavior is very lower for ACSxxx-6 and ACS110/ACS120 devices where the (dI/dt)c parameter is quite similar for both polarities.

Figure 8. ACS108-8 (dI/dt)c typical ability versus reapplied (dV/dt)c rate at T_j = 125 °C



For a 200 mA RMS current pump (see case 1 in Figure 8), the turn-off perform whatever the current sign is. The maximum turn-off delay is then one half-cycle (10 ms for 50 Hz mains frequency). On the other hand, for a 200 - 600 mA RMS pump (see case 2 in Figure 8) and for a 125 °C junction temperature, the switch-off is achieved when the current reaches zero with a negative sign. Therefore, in this case, the turn-off delay time can reach up to 20 ms for 50 Hz line frequency (Figure 9).

Figure 9. Turn-off delay for two different pump or fan RMS current



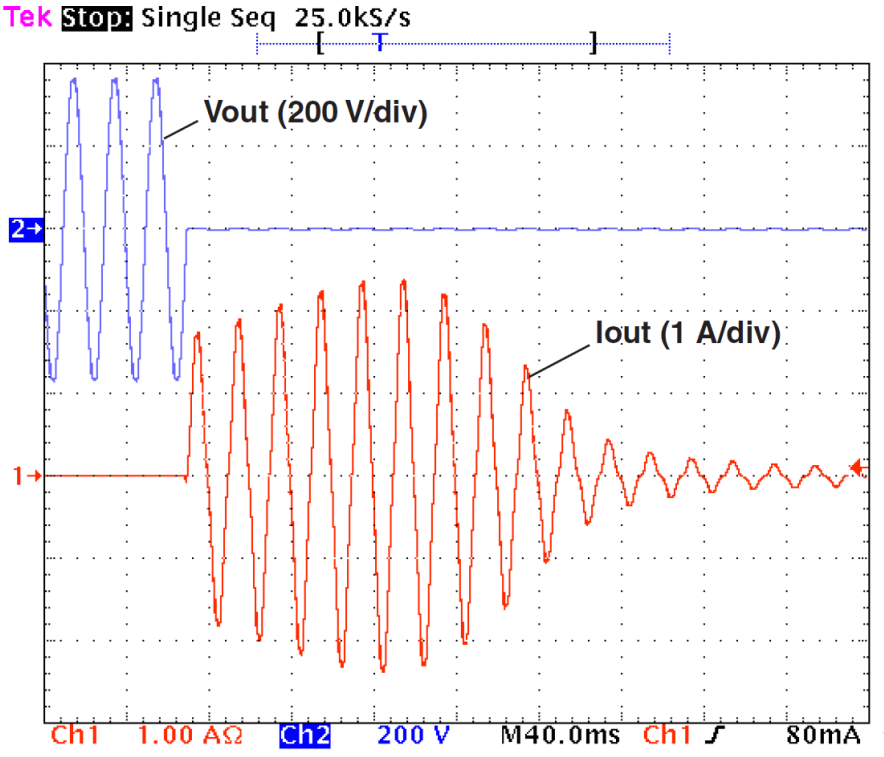
3 Resistive loads on/off control

3.1 Inrush current

In most systems, resistive loads are thermal effective. For example, light bulbs emit light when their filament is hot enough. New types of door-lock actuators have emerged in which the bolt move is due to a thermal expansion of a metallic part or a wax.

All these loads can be characterized by a very low resistance value in cold state. Consequently, when the switch is turned on, there is a high inrush current. For low power light bulbs, the inrush current lasts on average 10 ms. The worst scenario is in the case of thermal door-locks. Figure 10 shows a typical inrush current in such loads.

Figure 10. Inrush current in a 230 V thermal effective door-lock



3.2 Transient junction temperature

With such current shapes at turn-on, thermal calculation must be carried out to choose the right package or heat-sink so as to avoid exceeding the maximal junction temperature (125 °C). To perform the calculus, the current shape must be simplified. Let us work on the hypothesis that the current average waveform of Figure 10 is similar to a 2 A peak 0.18 s time long sinus shape.

Then, the average conduction and gate current losses in the ACS are given by the following relationship:

$$P_{AV} = r_d I_{RMS}^2 \frac{2\sqrt{2}}{\pi} + V_{gt} I_g \quad (4)$$

Then, according to ACS108-8 specifications, we find: Pav = 1.76 W.

For a tp long dissipated power pulse, the peak junction temperature ($T_{j\ peak}$) is given by equation 5, where T_{jo} is the initial T_j value.

$$T_{jpeak} = T_{jo} + Z_{TH}(t_P) \cdot P_{AV} \quad (5)$$

Since the thermal impedance values at 0.18 s for TO-92 and SOT223-2 packages are 22.5 and 6.5 °C/W respectively, it can be said that the junction temperature elevation, at the end of the inrush current period, is 40°C for a TO-92 package and 11.5 °C for a SOT223-2L package.

So, the maximal junction temperature before a door lock switch-on should be at most 85 °C for the ACS108-8SA (TO-92) and 113.5 °C for the ACS108-8SP (SOT223-2L), to keep a T_j peak below T_j max (125 °C). For washing systems, as the door lock start may appear at the beginning of a washing cycle, we suppose that T_{jo} equals at worst the maximal ambient temperature, that is, 70°C. So, in this respect, both ACS devices are convenient for door lock operation.

4 Electromagnetic compatibility standards

4.1 IEC 61000-4-5 standard

4.1.1 Standard requirements

The IEC 61000-4-5 standard has been established to check if systems can always work after there has been a voltage surge super-imposed to the mains. A standard voltage waveform has been chosen which embodies typical overvoltages due to thunder or disconnection of running inductive loads from the line.

Two kinds of surges must be applied:

1. Line to Ground surge: in this case the maximum voltage surge is 4 kV (for an aerial power network), but the energy is absorbed by the Y2 capacitors (connected between lines and ground) of the mains filter.
2. Line to neutral surge: in this case the maximum voltage surge is 2 kV (for aerial power network, N.B: 1 kV is required for the public power network) and is applied across the power device and the load controlled by this one.

A Line to neutral overvoltage is then:

1. Entirely absorbed by the load if the power switch is ON
2. Entirely held by the semiconductor device if it appears while the switch is at off-state.

As the Line to neutral surge can appear at peak mains voltage, the overall amount of voltage can reach 2.4 kV. This is higher than the break-down level of the silicon devices used in appliances. Then, to prevent component destruction, designers use a varistor connected across silicon devices. The overvoltage is limited below the breakdown level of the power semiconductor and the surge energy is absorbed by the metal-oxyde component.

4.1.2 ACS behavior during IEC 61000-4-5 test

When a surge appears when an ACS is OFF, the mains overvoltage is first clamped by the device. But an excessive energy surge can raise the ACS current above its breakover level. Then, the switch turns on in break over mode. Such an event is particularly stressful on the semiconductor moreover when the current and its rates of increase are both high. The worst case occurs for ACS driving low-resistance, non inductive loads.

For example, Figure 11 and Figure 12 have been recorded with a thermal active door lock system at low temperature. The 2 kV surge is super-imposed to the 230 V - 50 Hz mains and synchronized with its peak value, as shown on Figure 11, and Figure 12, highlights the device turn-on in this mode. As the load was previously off, its resistance is cold and equals 150 Ω. In this case, the current rises at a rate of 100 A/µs and reaches 15 A. Such transient surges would damage triacs, but not ACSs, which are designed to turn-on in breakover mode. No more varistor is then needed in parallel across ACSs unlike triacs. The difference between ACS and triac + varistor is that, with the ACS, the load is switched on during a half or one mains cycle. This can be accepted as such events happen a few times in the system's life.

Reliability tests are carried out on production batches to check the ACS robustness towards IEC 61000-4-5. A standard surge generator is used directly across a load and an ACS. The load is a 150 Ω resistor, including a 3 µH parasitic inductance, to simulate a cold door-lock.

The applied surge is fixed at +/- 2.4 kV in order to be equivalent to a 2 kV overvoltage applied at the peak mains voltage, with the same bias.

Figure 11. 2 kV surge on the mains (IEC 61000-4-5 test)

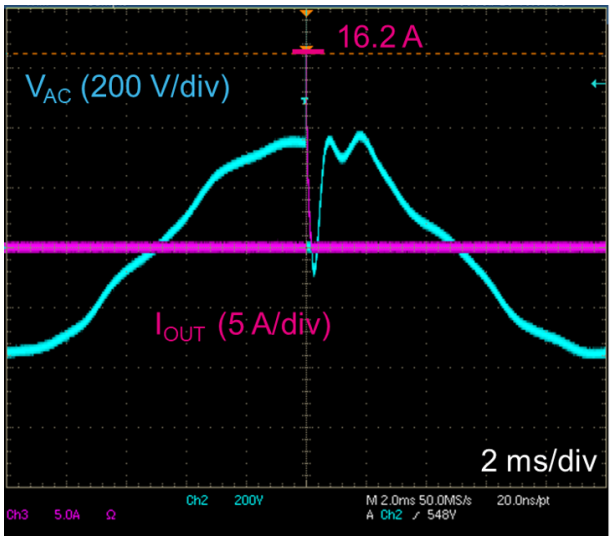
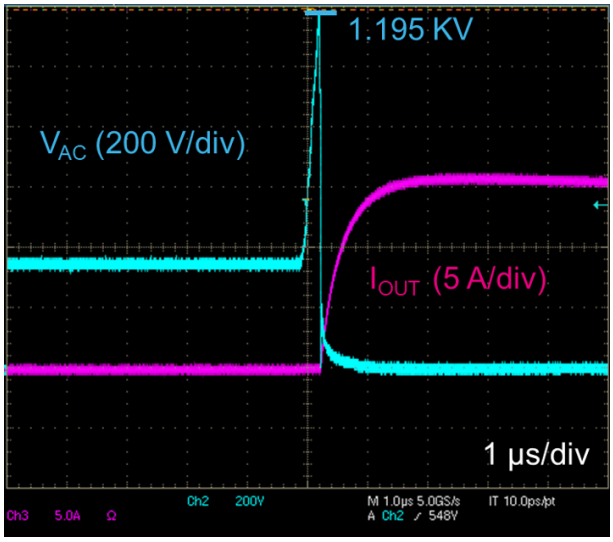


Figure 12. ACS breakdown zoom (IEC 61000-4-5 test)



4.2 IEC 61000-4-4 standard

4.2.1 2.1: Standard requirements

For the IEC 61000-4-4 tests, two different stressing ways are demanded. One is to apply the bursts to the Line, neutral, or Ground through 33 nF capacitors. In this case, the bursts are entirely absorbed by the mains filter, which is always present at the input of electronic systems. The second IEC 61000-4-4 stressing mode is to apply the bursts through a typical 100 pF capacitor (realized by an aluminum sheet), directly to the I/O ports of the system.

The I/O port test is in fact required for systems where there are control wires, as for computers (wires between keyboard and central unit). But appliance manufacturers apply a similar test to check if their products can withstand fast voltage transients.

The standard requires that for burst voltages up to 2 kV, the system must operate without problem. However, the triacs can turn-on due to high dV/dt rates. In this case, a snubber must be added to smooth these rates. Designers must then manage with the following trade-off:

1. Reduce dV/dt rates: the snubber capacitance must be high and the snubber resistance must be low
2. Reduce the dI/dt rate at turn-on: the snubber capacitance must be low and the snubber resistance must be high

4.2.2 Snubber removal thanks to ACSs

I/O tests have been carried out on an electronic board including an ACS108-8SA. The system under test is embodied by this board. The I/O wires are then the OUT pins of the ACS cell (which is connected to the loads), plus the Line and neutral wires. The trial diagram is shown in Figure 13.

Figure 13. IEC 61000-4-4 test synopsis

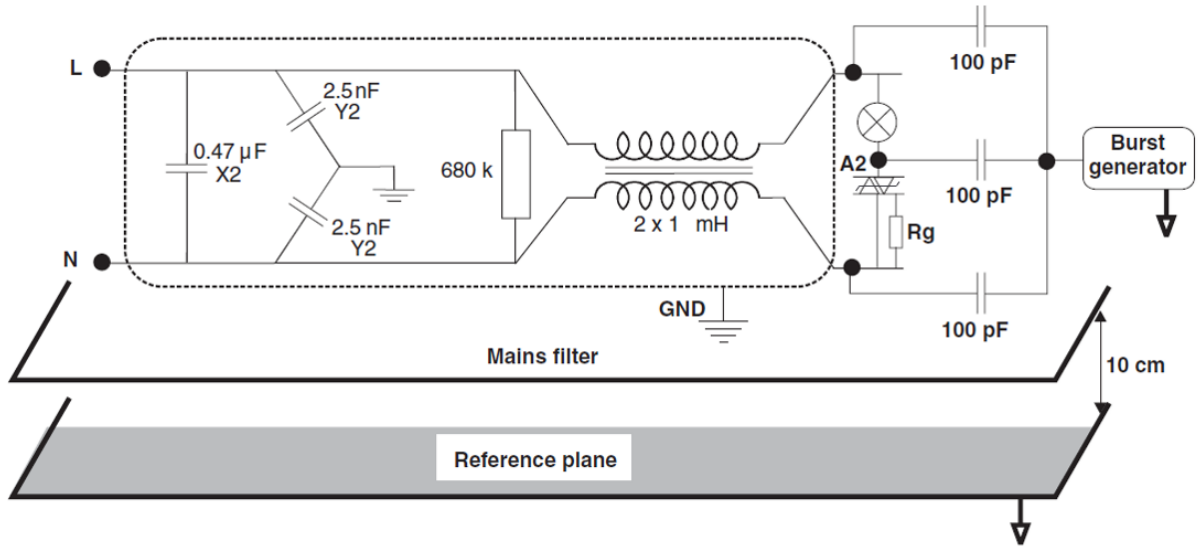
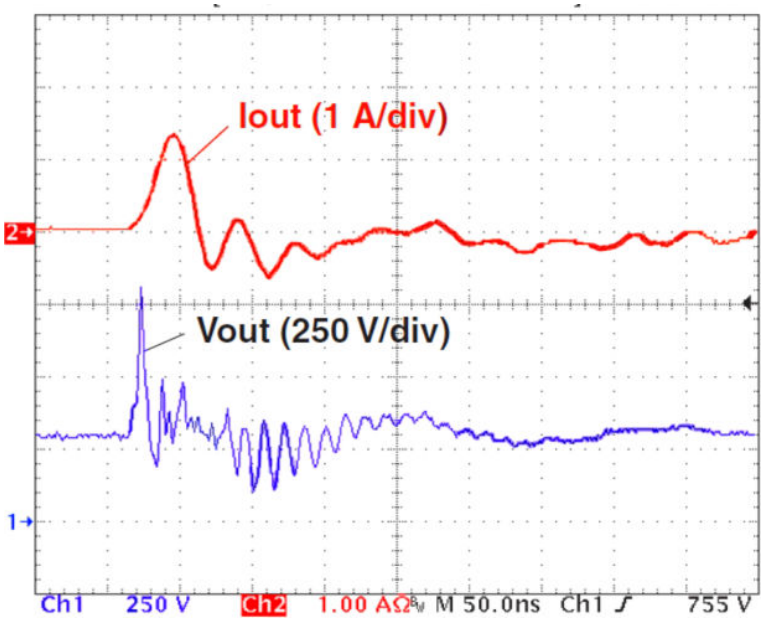


Figure 14 shows the OUT-COM voltage measured during a 2 kV IEC 61000-4-4 test (1 kV is required for a public power network). We see that in spite of capacitive current due to high dV/dt rates, the ACS does not turn-on. The semiconductor switch withstanding to IEC 61000-4-4 depends on its dV/dt capability. ACS devices present dV/dt characteristics 10 times greater than both the same current and sensibility ratings triacs. For example, a 10 mA maximum 0.2 A I_{GT} ACS has a minimum dV/dt capability of 500 V/µs (at T_j = 110 °C).

It can also be seen that the ACS voltage overflows its breakdown value given for a 50 Hz sine wave (810 V is reached in spite of the 650 V breakdown value). In fact, the voltage rate of increase is so high that the silicon device has not enough time to begin to clamp. A higher value than its V_{CL} value can then be reached.

Figure 14. IEC 61000-4-4 test on ACS108-8 cell for a 2 kV burst



To sum up, it can be said that ACSs, thanks to their high dV/dt capability, improve the overall electronic board robustness towards fast line transients without any snubber. But it must be kept in mind that the mains filter Y2 capacitors also play a role in sustaining the IEC 61000-4-4 tests, by derivating some part of the bursts energy. The typical values of these capacitors are 2.2 nF.

5 Conclusion

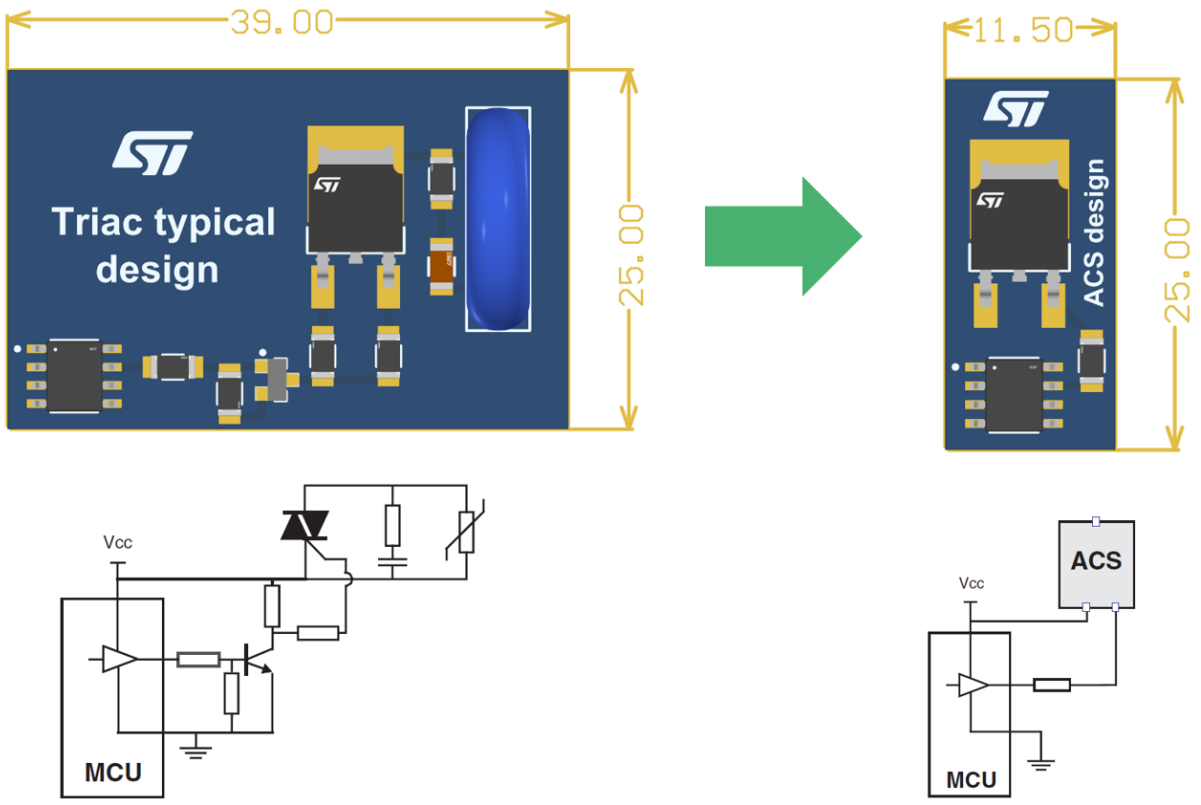
ACS retains the well-known advantages of the triac (high AC voltage blocking capability, current bidirectionality) and adds high over-voltage robustness and the increased reliability and compactness that appliance manufacturers now need.

Due to to the clamping capability and robust break-over characteristics of the ACS structure, the protection circuits that are usually connected in parallel with the triacs, are no longer required. The varistor removal increases automatically the reliability of the electronic board. And the snubber removal allows designers to be free with the dV/dt at off state and dI/dt at turn-on trade-off when choosing an R-C circuit.

In addition, the triac gate-drive transistor and its associated resistors are also redundant because ACS devices have built-in logic level drive circuits that allow the power switch to be safely driven from any MCU output pin capable of sinking 20 mA without over-stressing the micro-controller output. Hence, the typical component count falls from eight with triacs, down to two with ACSs (see Figure 15).

The new ACS devices represent a real breakthrough in the design of power switches for home appliances. The enhanced performance, for example their robust off-state and logic level drive, allied to their inherent compactness open new perspectives in the design of compact and reliable electronic power controllers.

Figure 15. Component count reduction thanks to ACS



Appendix A References

Table 2. reference name and description

Ref. name	Description
[1]	P.Rault, "Triacs for Home Appliances: present and future", PCIM forum, Honk Kong, pp. 57-65, 1998.
[2]	AN302, Thyristors and TRIACs: holding current - an important parameter.
[3]	AN439, Snubberless and logic level triac behavior at turn-off.
[4]	SCR Manual, General Electric, 6th Edition, 1979.

Appendix B STEVAL-GLA001V1 demoboard

Figure 16 shows the electronic diagram of a demonstration board used to illustrate ACS / STM32 compatibility The mains features are:

- Insulated control of three different AC switches used to drive AC loads up to - 1 kW (230 Vrms) for residential appliances
- Interface with STM32 Nucleo-64 development board
- Three control modes available thanks to STM32 Nucleo-64 firmware (continuous - or pulse gate current, timer option and phase control)
- Easy to configure through user-friendly interface
- Compatible with any external microcontroller
- Input voltage range: 90 VAC to 265 VAC 50 / 60 Hz
- Operating temperature: 0 °C to 60 °C - 5 V and 3.3 V insulated power supply
- Low standby power losses (< 300 mW)
- Criteria A at 2 kV IEC 61000-4-4
- Criteria B at 4 kV IEC 61000-4-4
- RoHS compliant

Figure 16. STEVAL-GLA001V1 block diagram

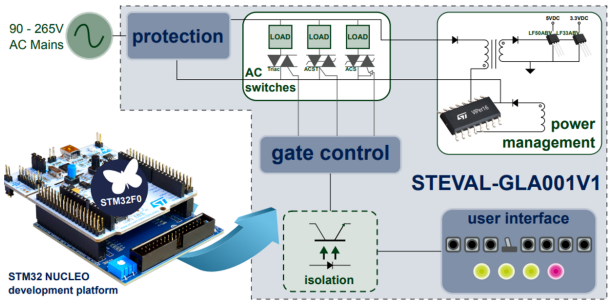
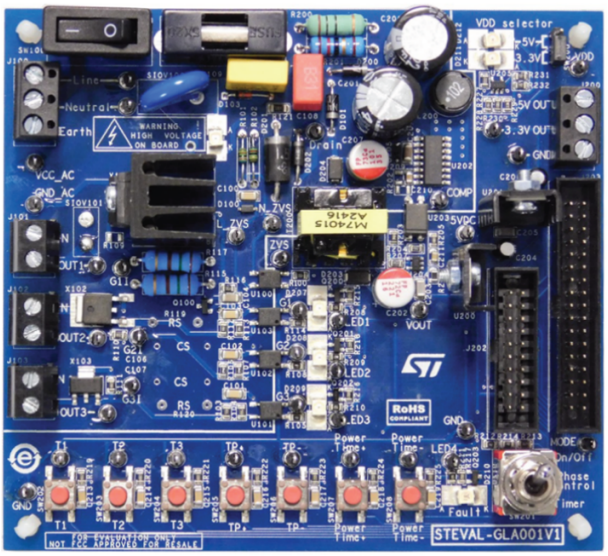


Figure 17. STEVAL-GLA001V1 board layout



Appendix C ESD diode conduction due to kick-back

An over-voltage can appear across the gate and COM (or A1 for triacs) terminals at high turn-on di/dt rates. This effect is called the "kick-back". It is due to the high density current at turn-on which causes high conduction voltage drop. Since the conduction begins around the gate area, the forward voltage is in part applied to the gate.

This gate spike is clamped by the micro-controller internal electrostatic discharge (ESD) diodes, which can be damaged if conduction lasts for too long.

In order to prevent ESD diodes conduction, their voltage must remain negative. When considering Figure 1 at ACS turn-on, i.e. when the push transistor M1 is off and the pull transistor M2 is on, a circulating current never occur through D2 if the current iR remains positive. This yields Eq. (6).

$$R \cdot i_R = -V_{M2} + V_S + V_g > 0 \quad (6)$$

As M2 is conducting, its voltage drop can be neglected. Thus, the previous relation gives:

$$V_g > -V_S \quad (7)$$

If D1 conducts, this means that the supply voltage is held by M2, neglecting D1 drop voltage. This MOS transistor is thus in a linear mode. Its current equals its saturating level, called isat. Now, since isat current is necessarily higher than the V_S/R ratio (in order to secure the microcontroller operation), we can write the following relationship :

$$V_{D1} = V_g - R \cdot i_{SAT} > V_g - V_S \quad (8)$$

A sufficient condition to ensure that V_{D1} remains below zero is that V_g remains below V_s. This condition, plus Eq. (7), gives the following safety rule for no ESD diode conduction:

$$-V_S < V_g < +V_S \quad (9)$$

Figure 18. Kick-back test with ACS102

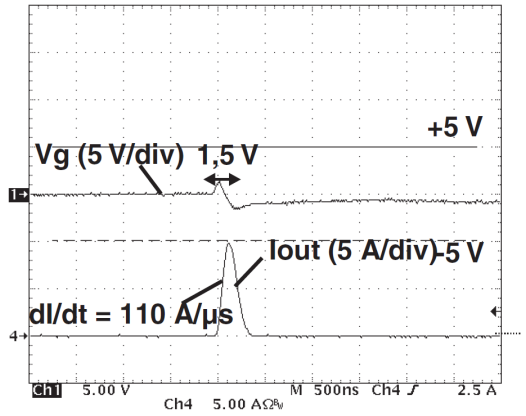
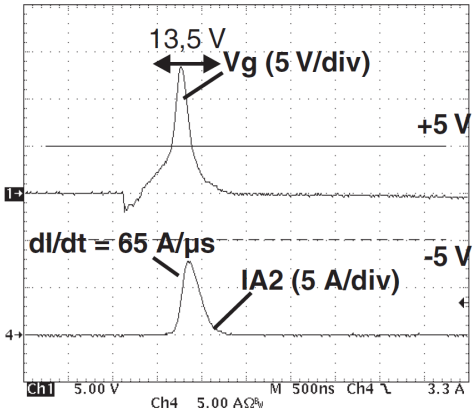


Figure 19. Kick-back test with Z0109 triac



To compare the kick-back effect of triacs and ACSs, a special test circuit has been defined. It consists on turning on the switch with a 10nF capacitor connected directly across the A1- A2 or OUT-COM terminals. The capacitor is charged at 300 V. Figure 18 and Figure 19 show the experimental results obtained with such a testing method, for a positive bias voltage.

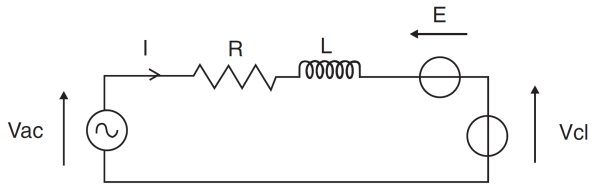
A Z0109 (0.8 A I_{RMS} 10 mA i_{gt} ST triac) doesn't fulfill with Eq. (9), for V_{GA1} voltage reaches 13.5 V with a 65 A/µs dI/dt rate. This is largely above the supply voltage. With the ACS102, the maximum V_g voltage is 1.5 V, and is still within the limits of Eq. (9) despite a dI/dt which is twice as big as with the Z0109. ACS / MCU interface would then be secured even at turn-on at peak mains voltage or on a short-circuit.

Appendix D How to calculate the junction temperature during clamping periods

D.1 Dissipated power evaluation

It should be kept in mind that the load inductive energy is not entirely absorbed by the die at clamping. Another part is dissipated by the Joule effect in the load resistor or absorbed by the mains. A way to accurately evaluate the clamping energy is then to estimate the ACS current waveform, versus the time. The energy is then calculated by integrating this waveform and the product of the clamping voltage along the turn-off period.

Figure 20. Electric equivalent circuit at clamping



Let us consider a typical AC load equivalent circuit shown in Figure 20. The load current during the clamping time is given by the following relationship.

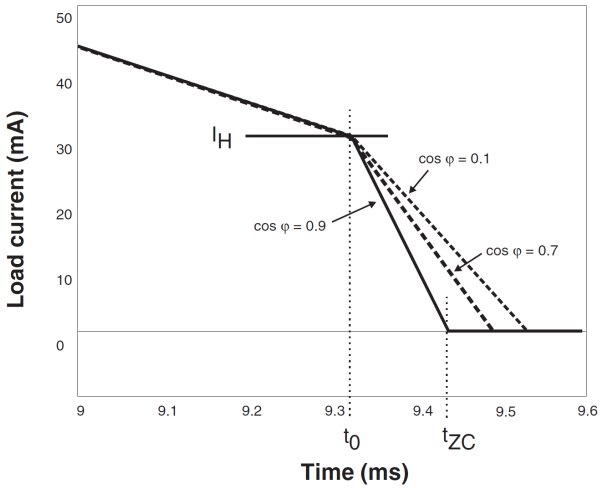
$$i\left(t\right) = \frac{V_{CL} + E - V_{AC}}{R}\left(e^{-\frac{R}{L}\left(t - t_0\right)} - 1\right) + i\left(t_0\right) \cdot e^{-\frac{R}{L}\left(t - t_0\right)} \quad (10)$$

It is difficult to evaluate the influence of E in a general way. Its sign depends on its phase towards the current and the value of the holding current. But, it can be said that the back electromotive force has little influence for most universal and synchronous motors in which impedances are high and E is close to zero. Furthermore, for all other loads, such as passive loads or asynchronous motors, the b.e.m.f E is null. For this reason, let us neglect its value. Let cosφ be the load power factor and V the RMS mains voltage. Since the clamping occurs near the zero crossing current, the value of the main voltage at t0, for a positive current, is given by the relationship Eq. (11).

$$V_{AC} = -V\sqrt{2} \cdot \left|1 - Cos^2\varphi\right| \quad (11)$$

Figure 21 shows the current waveforms calculated with such an hypothesis, and assuming that the holding current does not depend on the current rate of decrease. The junction temperature influence on the i_H and V_{CL} levels is also not considered. Then, $i(t_0)$, in Eq. (10), is equal to the i_H value given for a 25°C junction temperature (ex: around 30 mA for an ACS102-6 or an ACS108-8). The ACS clamping voltage is taken equal to 700 V. Calculations are carried out for 100 mA RMS loads with different power factors, and for a 230 V 50 Hz mains voltage.

Figure 21. Current waveform during clamping phase for 100mA / 230V RMS loads



Considering Figure 21, we can see that the load current is always inferior to a linearly decreasing current beginning at (i_H, t_0) point and ending at (0, t_{ZC}). Furthermore, the temperature elevation due to a rectangular power pulse is always superior to the one due to a decreasing triangular power pulse of same average value (see [3].).

So, a pessimistic way to calculate the junction temperature is to simplify the clamping losses shape by a constant power pulse of V_{CL}. I_H/2 value and t_{ZC}-t0 time long. The energy absorbed by the die during a clamping event (E_{CL}) depends on two ACS parameters (V_{CL} and I_H) and on the clamping duration:

$$E_{CL} = \frac{1}{2} V_{CL} I_H \left(t_{ZC} - t_0 \right) \quad (12)$$

D.2 Transient maximum junction temperature

The clamping time is given by Eq. (10), which gives way to the following one.

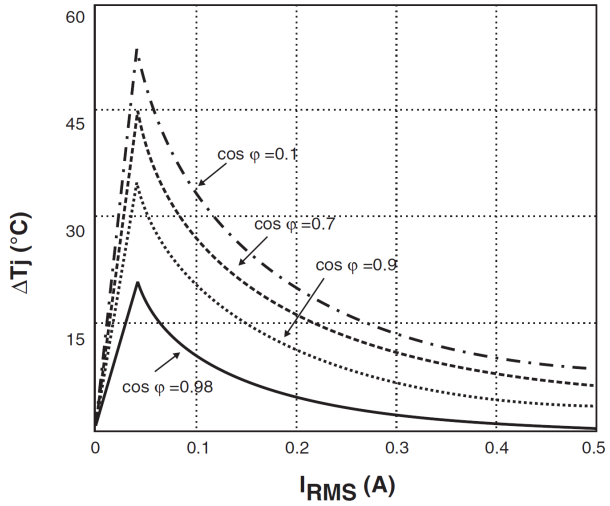
$$t_{ZC} - t_0 \frac{L}{R} \ln\left[1 + \frac{R}{V_{CL} + E - V_{AC}} i_H\right] \quad (13)$$

Neglecting the on-state dissipated power in front of clamping dissipated power, the junction temperature rise at the end of the clamping phase is:

$$\Delta T_j = Z_{TH}\left(t_{ZC} - t_0\right) \cdot \frac{1}{2} V_{CL} I_H \quad (14)$$

Figure 22 shows the maximum ΔTj reached for different load RMS currents and power factors. Calculations are similar whatever the package is (TO-92, DIL-20, SOT223), because in such a range of times, the Z_{TH} is only due to the die area. Note that ΔT_j first increases. On this curve part, the load peak current is lower than the iH level (taken equal to its worst value: 60 mA). So, when the load RMS current increases, the turned-off current increases too. When the load peak current becomes higher than i_H, ΔT_j decreases because of the load series inductance decrease (here the turn-off current is constant and equals i_H).

Figure 22. Supplementary temperature rise at clamping depending on load nature (for ACS102-6 or ACS108-8)



It can be concluded that, if the junction temperature was 125 °C before turn-off, the maximum transient temperature can reach 175 °C. As these events last less than one ms (refer to Figure 21), such junction temperatures can be permitted.

D.3 Repetitive clampings

To evaluate heating due to repetitive clampings, Eq. (15) can be used, assuming that the clampings occur at a constant period T and that the conduction losses can be neglected in front of the previous ones.

$$\Delta T_{rep} = \frac{1}{2} V_{CL} I_H \left[\frac{t_{ZC} - t_0}{T} R_{TH} + \left(1 - \frac{t_{ZC} - t_0}{T}\right) Z_{TH}\left(T + t_{ZC} - t_0\right) - Z_{TH}\left(T\right) + Z_{TH}\left(t_{ZC} - t_0\right) \right] \quad (15)$$

In practice T (above 1s) is very much higher than the clamping duration. Eq. (16) can then be simplified to the following one.

$$\Delta T_{rep} = \frac{1}{2} V_{CL} I_H \frac{t_{ZC} - t_0}{T} R_{TH} \quad (16)$$

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
10-Jun-1999	1	Initial release.
11-May-2006	2	Reformatted to current standard. *Figure 1.*, *Figure 6.*, *Figure 17.*, and *Figure 18.* updated.
28-Mar-2024	3	Updated Figure 2, and Figure 3. Inserted Section 1.3: ACS108-8SP. Updated Figure 5, Figure 6, and Figure 7. Removed "*Light bulbflashhover*" chapter. Updated Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Appendix B: STEVAL-GLA001V1 demoboard, Figure 18, and Figure 19. Minor text changes.

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