



life.augmented

# **ST50V10200\_REV1\_0**

## **Model information**

**Keysight Advanced Design System Model  
Generic Netlist Model**




STModelSimulation

STMicroelectronics

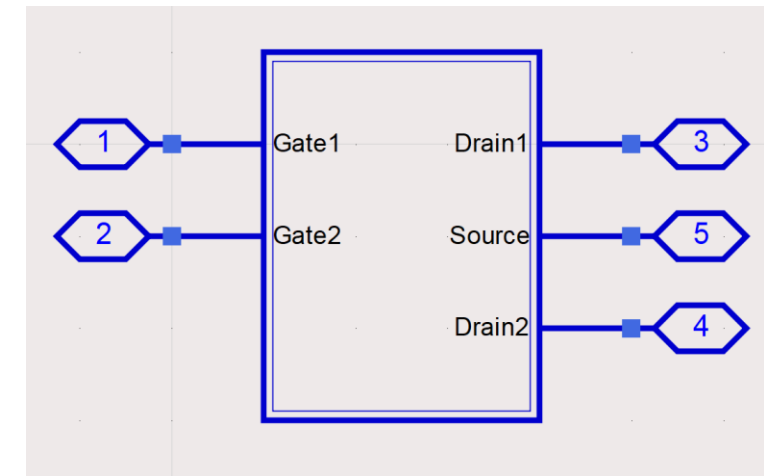
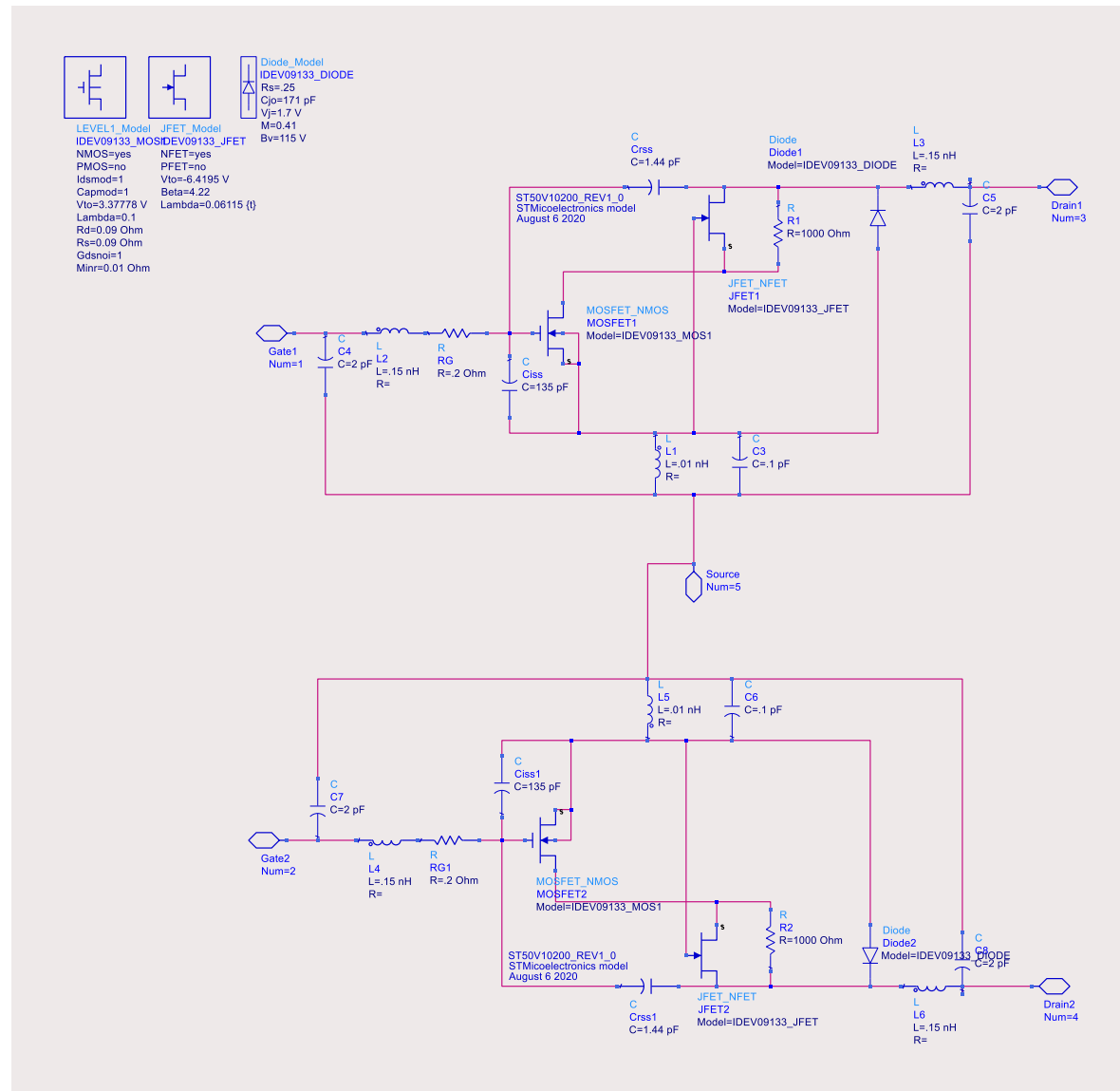
August 6 2020

 ST50V10200\_rev1\_0\_wrk.zip



 GenericNetlist  
 README  
 ST50V10200\_rev1\_0\_wrk

# Model configuration



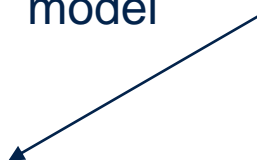
# Generic netlist

```
*ST50V10200_rev1_0 ONE SIDE
*8/6/2020
*STMicroelectronics
*port 1 = GATE , 2 = Drain , 3 = Source
*
.SUBCKT ST50V10200_oneside 10 20 30
LGATE 10 11 .15N
RGATE 11 12 .2
CG 10 30 2P
CRSS 12 17 1.44P
CISS 12 14 135P
LS 14 30 0.01N
CS 14 30 .1P
R 17 13 1000
LD 17 20 .15N
CD 20 30 2P
MOS 13 12 14 14 mos_9133 L=1uM W= 133mM
JFET 17 14 13 jf_9133
DBODY 14 17 d_9133

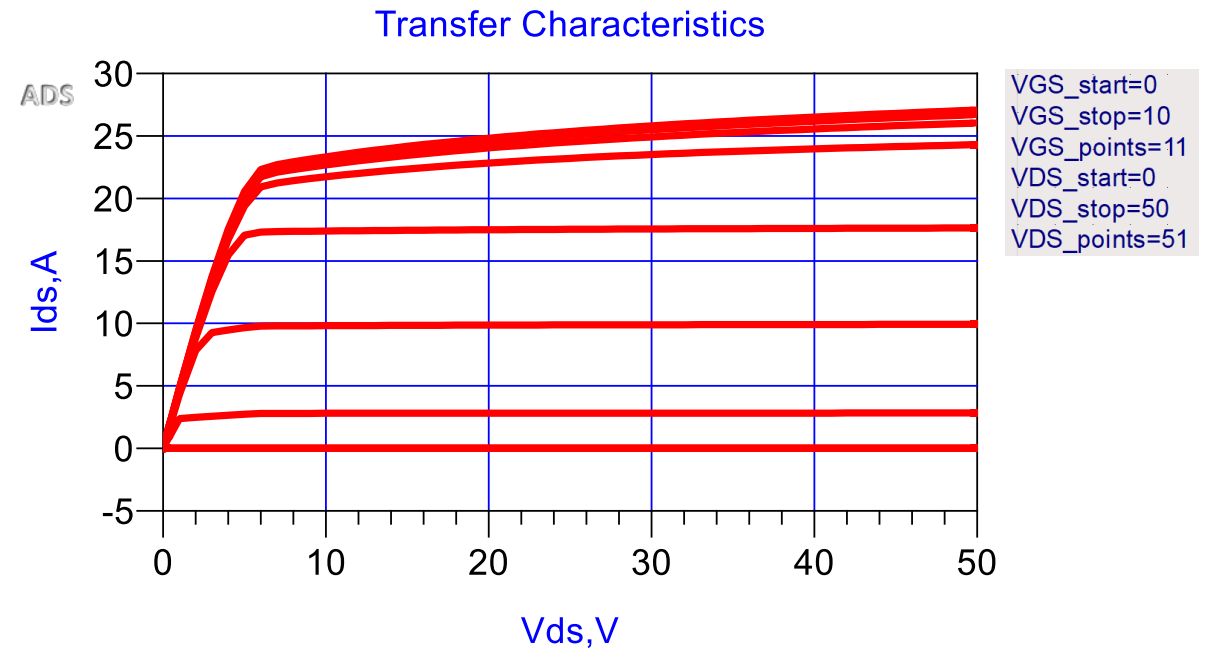
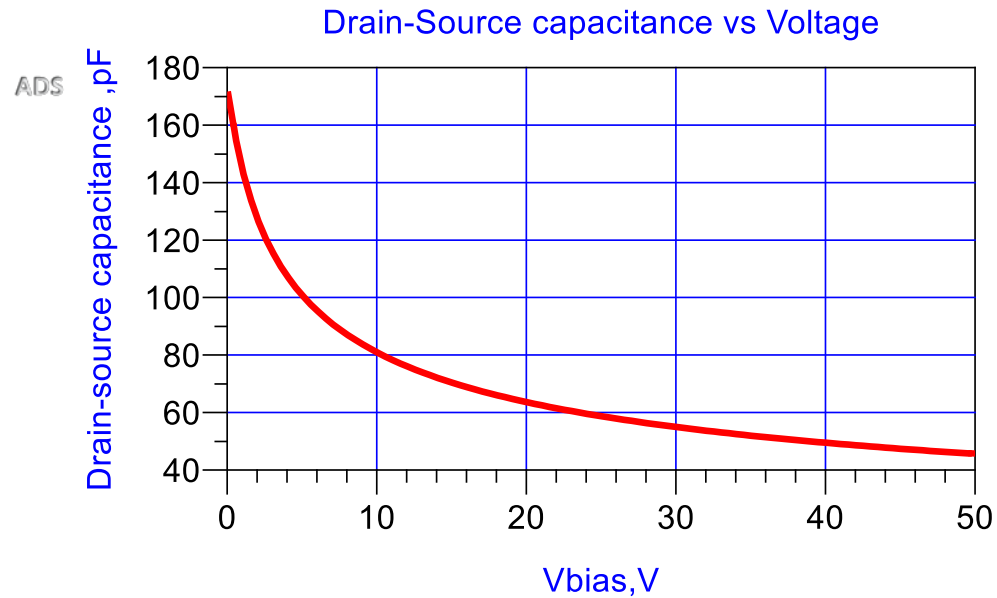
.MODEL mos_9133 nmos (vto=3.37778 KP=0.00020298 LAMBDA=0.1 RD=0.09 RS=0.09)
.MODEL jf_9133 njf (VTO=-6.4195 BETA=4.22 LAMBDA=.06115)
.MODEL d_9133 d (CJO=171p RS=0.25 VJ=1.7 M=0.41 BV=135)

.ENDS
```

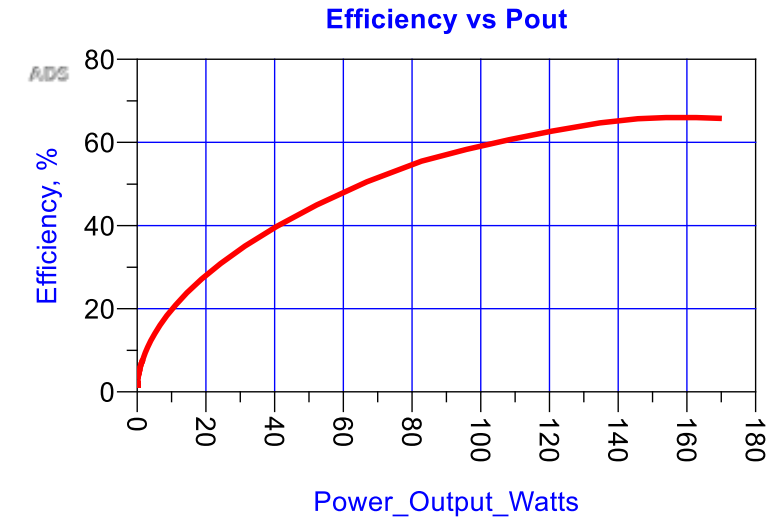
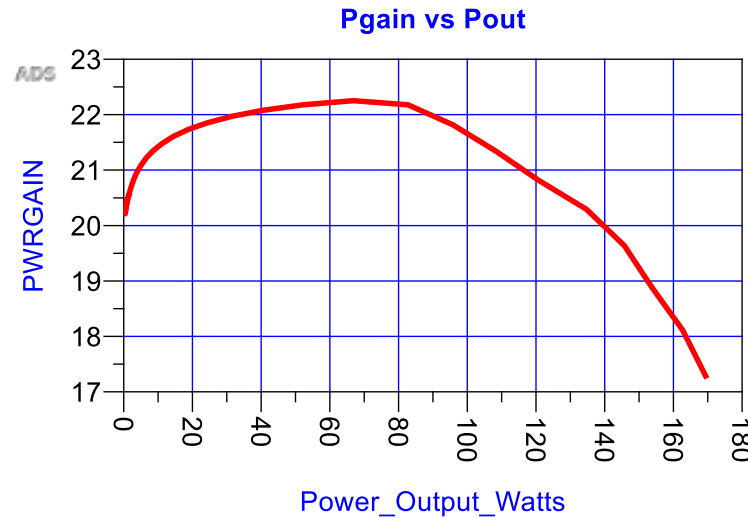
When using this netlist  
in ADS you may need to  
add Minr=0.01 ohms  
within the level1 mos  
model



# Example simulations one side



# Example simulations, 1 GHz one side

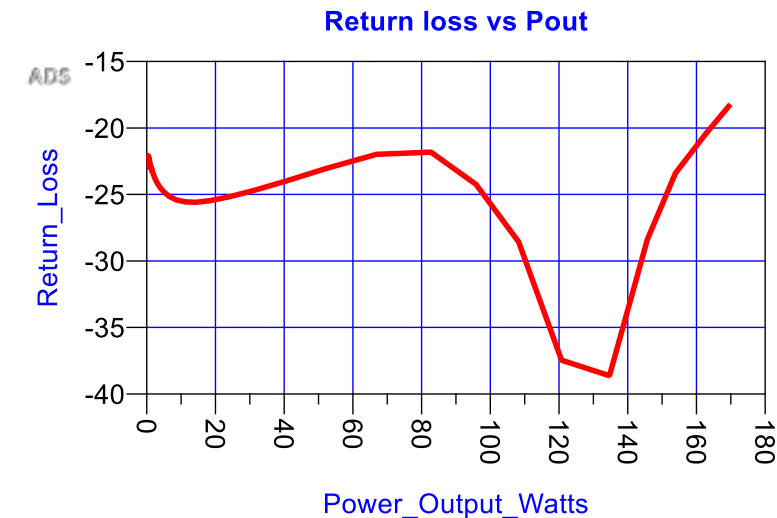


**Zin**

RF_freq	Rs	Xs
100.000	0.460	-9.129
200.000	0.417	-4.489
300.000	0.372	-2.886
400.000	0.359	-2.066
500.000	0.351	-1.511
600.000	0.345	-1.149
700.000	0.356	-0.901
800.000	0.337	-0.684
900.000	0.316	-0.493
1000.000	0.296	-0.323
1100.000	0.278	-0.168
1200.000	0.262	-0.023
1300.000	0.247	0.114
1400.000	0.233	0.246
1500.000	0.220	0.374

**Z drain load**

RF_freq	Rs_load	Xs_load
100.000	9.392	2.535
200.000	7.716	4.131
300.000	5.950	4.714
400.000	4.509	4.672
500.000	3.442	4.345
600.000	2.672	3.921
700.000	2.116	3.483
800.000	1.708	3.067
900.000	1.404	2.682
1000.000	1.172	2.330
1100.000	0.993	2.008
1200.000	0.852	1.713
1300.000	0.739	1.441
1400.000	0.647	1.189
1500.000	0.572	0.954



# Thank you