

SD3933  
Model  
using SD3931-10

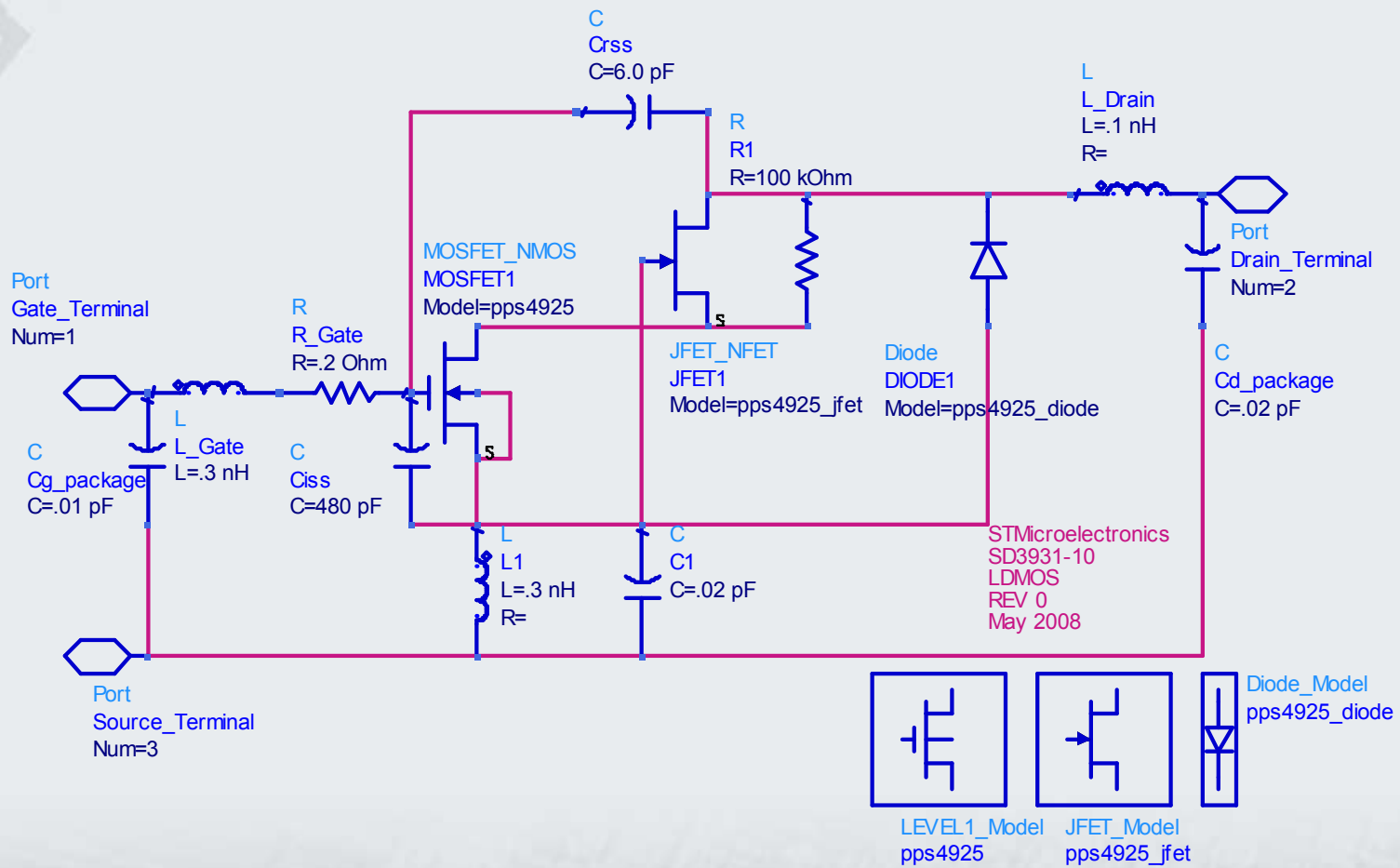


Quakertown , PA  
Qtn-jp-275-rev0  
August 15, 2008

## SD3933 model description

- SD3933 model
  - SD3931-10 Parallel with SD3931-10
  - Series Gate Resistance 2.08 OHM with each SD3931-10





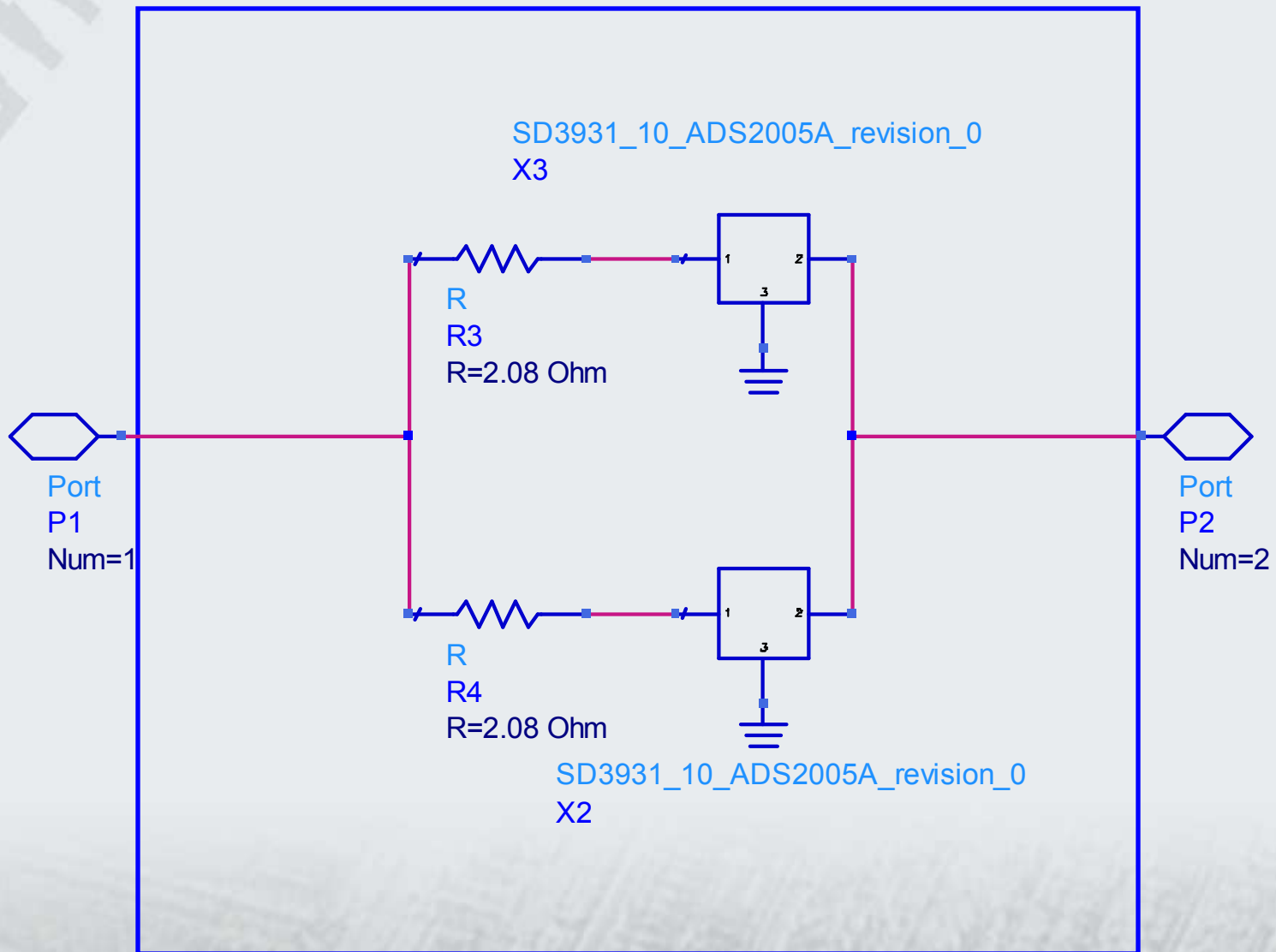
1/2 SD3933



- \* Vertical DMOS , Low Rds(on) process patent numbers US6750512,EP1296378
- \*Large Signal Model REVISION 0 jprit May 29 2008
- \*STMicroelectronics
- \*RF Product Development and Characterization
- \*Quakertown,PA,USA
- \*node 10 = Gate
- \*node 20 = Drain
- .SUBCKT sd3931/10 20 10 30
- lg 10 11 0.3N
- rg 11 12 0.2
- cg 10 30 0.01P
- crss 12 17 6P
- ciss 12 14 480P
- Ls 14 30 0.3N
- cs 14 30 0.02P
- R 17 13 100K
- ld 17 20 .1N
- cd 20 30 0.02P
- MOS 13 12 14 14 pps4925 L=.2u w=0.925
- JFET 17 14 13 pps4925j
- DBODY 14 17 pps4925d
- 
- .MODEL pps4925 nmos (vto=2.5 KP=0.71E-6 LAMBDA=1.0 RD=0.12 RS=0.12)
- .MODEL pps4925j njf (VTO=-5 BETA=3.26 LAMBDA=3)
- .MODEL pps4925d d (CJO=1050p RS=0.25 VJ=0.6 M=0.4 BV=260)
- .ENDS

## 1/2 SD3933 NETLIST





SD3933 MODEL = (SD3931-10 x 2) + 2.08 OHM resistors



**HARMONIC BALANCE**

HarmonicBalance  
HB1  
Freq[1]=RF\_freq MHz  
SweepVar="Pin"  
Start=10  
Stop=29  
Step=1

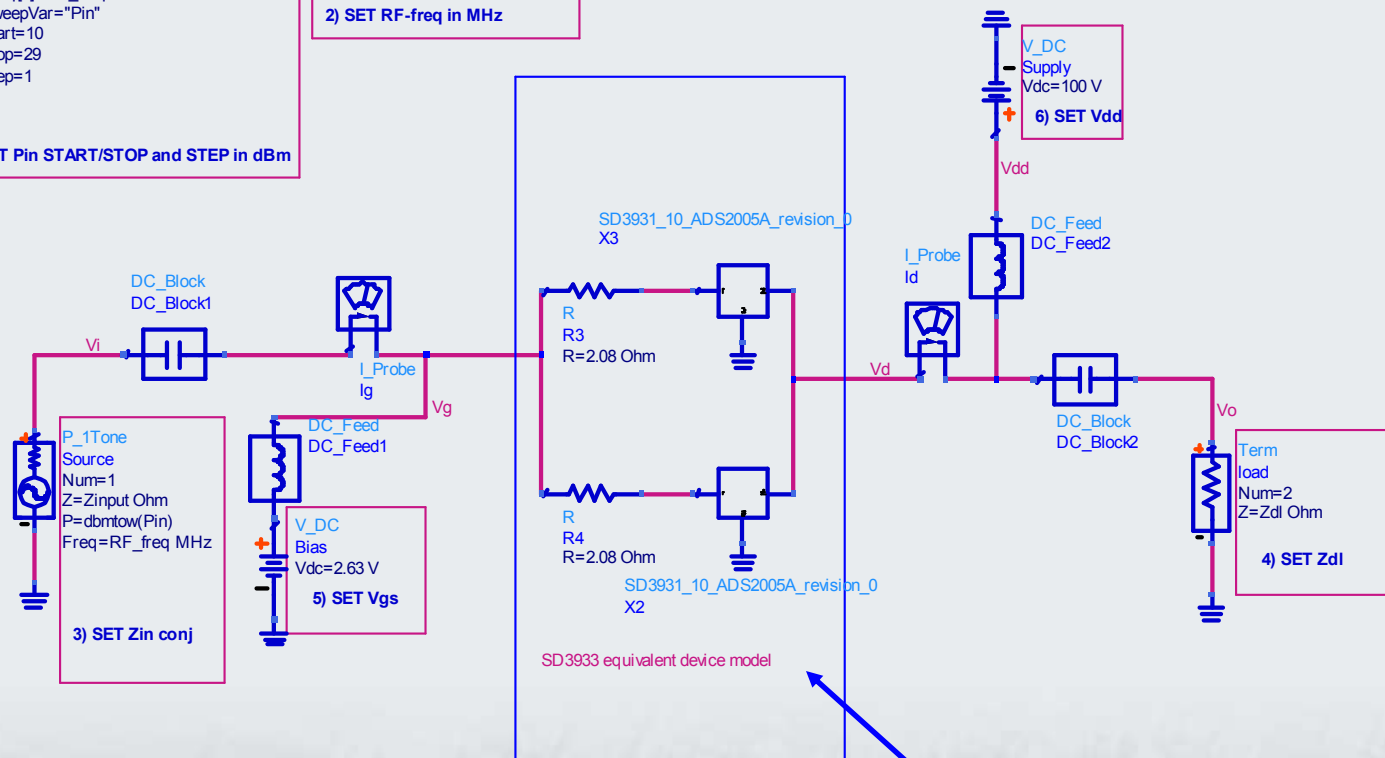
1) SET Pin START/STOP and STEP in dBm

**VAR**

VAR1  
RF\_freq=30  
Pin=0  
Zdl=(7+j\*7.5)  
Zinput=(2+j\*2.5)

2) SET RF-freq in MHz

STMicroelectronics  
ADS2008  
RF LARGE SIGNAL template\_REV\_0  
John Pritiskut ch\_ST\_QUAKERTOWN  
August 15 2008

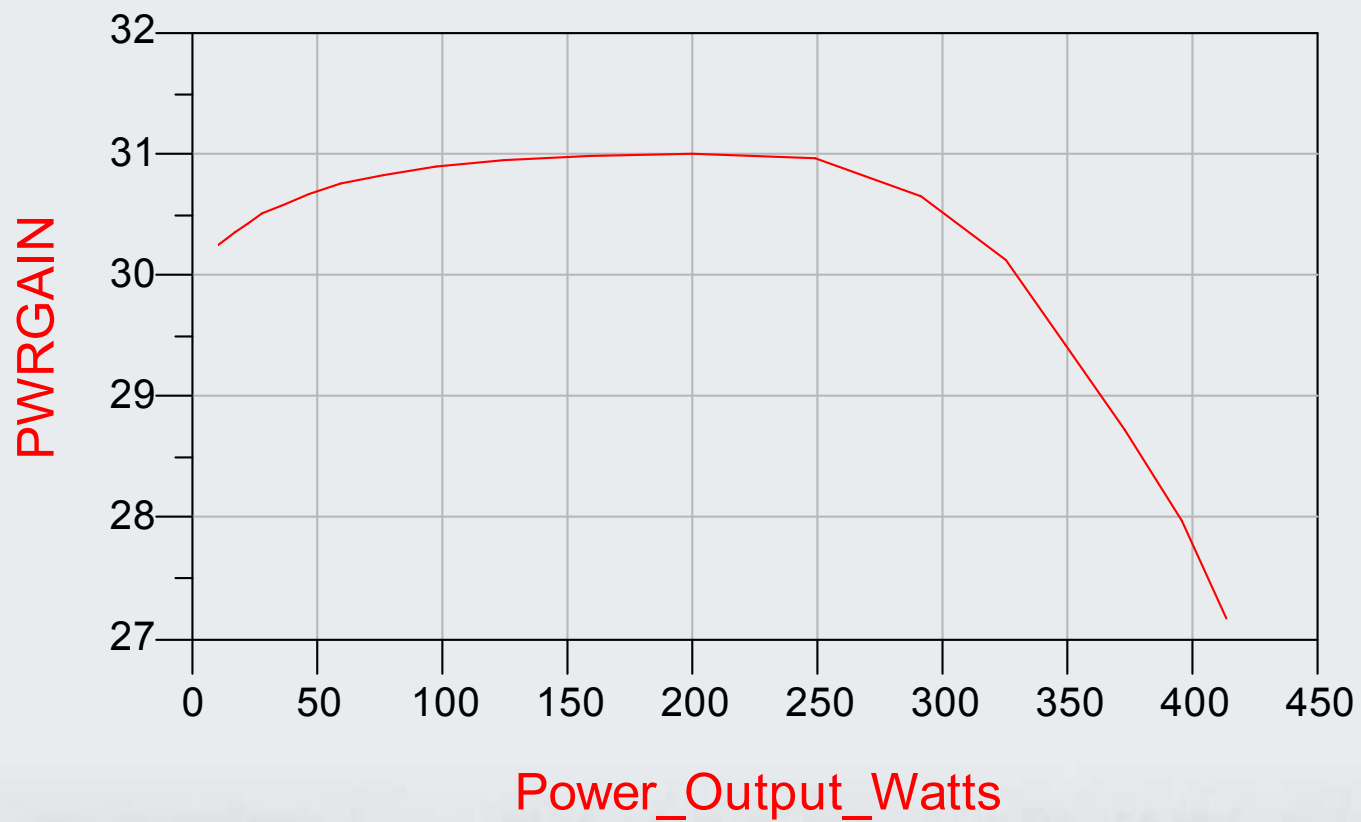


Large signal ADS circuit

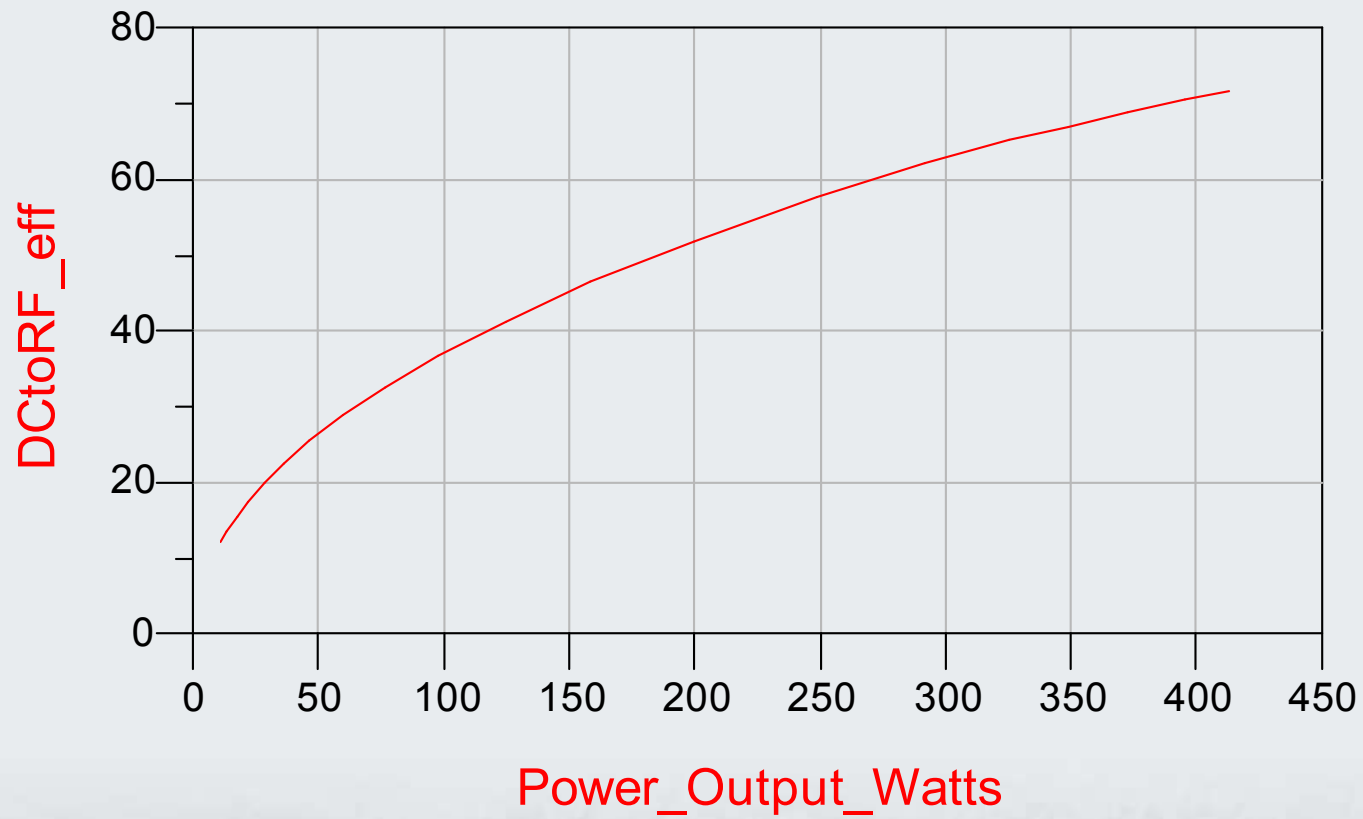
SD3933 Equivalent  
model



**Pgain vs Pout**



## Efficiency vs Pout



**Return loss vs Pout**

