Embedded Select in Trench Memory (eSTM), best in class 40nm floating gate based cell: a process integration challenge

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***Abstract*—** This paper discusses an innovative architecture of charge storage NVM cell, which outpaces state-of-the-art in term of bit-cell area. This new concept of memory cell is used today in production for microcontrollers. After cell architecture and activation description, we will present process flow integration challenges, process optimizations and single cell characterizations.

I. INTRODUCTION

The embedded non volatile memory based microcontrollers (eNVM MCU) market is growing very fast thanks to the increasing demand on general purpose (GP), automotive (Auto), internet of things (IoT) and secure (SC) applications. These applications require a scalable eNVM cell with high cycling capability, good retention and low power consumption on a wide range of temperature. Many emerging NVM cells are under development for advanced nodes (MRAM, PCM, RRAM) but charge storage cells remain the most used since decades for their simpler process and proven reliability.

Table I compares performance and scalability of various charge storage/trapping eNVM cell. Today, despite its more complex process, split gate eNVM cell family is the preferred solution in 40nm node. The presence of select gate allows better performance in term of power consumption during write operations, but also NVM macrocell optimization (area gain and simpler erase operation management) [1-4]. In this paper, we present a new highly reliable and scalable 40nm 1.5T cell. This NVM cell, called Embedded Select in Trench Memory (eSTM cell), has been developed to optimize microcontroller's area, cost and performance versus 1T NOR cell. eSTM presents the advantages of split gate cell with a very good scalability and reliability performances.

II. CELL ARCHITECTURE DESCRIPTION

A. Cell architecture

e-STM cell is a Flash NOR cell formed by a conventional 1T cell coupled with a vertical select transistor (Fig.1). Being vertical, select transistor channel length can be adjusted to sustain very low leakage level, even at hot temperature, without impacting bitcell area which is the more aggressive eNVM cell in 40nm node (0.049µm²) [5]. The cell is placed on Pwell isolated from bulk thanks to an n-iso buried implant that plays also the role of source plate. Vertical select transistor is common for odd and even cell. Cell selection is performed by selecting odd or even Bit Line (BL) and the select transistor word line (WL). The layout of the e-STM cell is pictured in Fig.2. CG and vertical select transistor are not self-aligned. We have studied the cell-to-trench distance impact on programming efficiency and demonstrated that working window is larger than alignment tolerance.

B. Cell operations

eSTM cell is erased by Fowler-Nordheim (FN) tunneling and programmed using hot electron mechanism similar to source side injection (SSI). As in a conventional 1T NOR flash, FN erase is obtained by generating high electric field across tunnel oxide using high voltage (HV) on CG and bulk terminals.

eSTM programming is performed using fast and low power mechanism enabled by the 1.5T architecture [6]. Efficient programming is obtained by polarizing the vertical select trench transistor in low inversion regime to limit current consumption and generate hot carriers (impact ionization in the pinch-off region as shown on Fig.3). Electrons move toward the tunnel oxide interface, and those having sufficient energy are injected into the floating gate across tunnel oxide thanks to the vertical electric field. Injection current obtained by TCAD simulation shows a wide injection distribution along the tunnel oxide with a clear peak on the cell source side (Fig.4). This wide injection distribution is attributed to a spread of electrons in the region between tunnel oxide and select transistor.

Thanks to the very low select transistor off current, we can tolerate depleted cells (negative erase Vt distribution). This allows to perform read operation by keeping CG grounded and suppresses read disturb mechanism [7]. Table II shows bias applied for each operation.

III. PROCESS

A. Process flow

The eSTM specific trench definition steps are performed at the beginning of the flow. Active, Niso, HV and NVM well implants are defined similarly to a 1T NOR cell. Select Trench steps are then inserted in the flow prior to the HV & Tunnel oxide definition. The trench transistor process flow can be

described as follow (Fig.5). First a nitride layer is deposited and will be used as polishing stop layer. Then, trench is patterned. It is perpendicular to the active layer and therefore crosses both silicon active and oxide Shallow Trench Isolation (STI) regions. (Fig.6). The trench depth control is a technological challenge of this integration. However, trench depth process window is comfortable enough for manufacturing, as presented in Fig.7, showing impact of trench depth (select length) on select transistor parameters. Minor saturation and leakage current impacts are observed with 5% of variation on select gate depth. Then gate oxide grows along sidewalls and bottom of the trench. Sidewalls roughness and steepness are critical to ensure maximum gate oxide lifetime performance. Trench filling with in situ doped polycrystalline silicon (poly0) deposition allows to generate the transistor gate. Chemical and Mechanical Polishing (CMP) is then performed to remove poly0 surplus. Last step is dry etch of poly0 in order to adjust height (recess) in the trench. Then rest of eSTM process flow is similar to the 1T NOR one's.

One of the challenge of integrating vertical select transistor in the memory process flow was to maintain manufacturing compatibility with the 1T NOR cell platform for IPs re-use and time to market speed up. Fig.8 shows a perfect parametric alignment of digital and HV MOS for both 1T NOR and eSTM technologies.

B. Process trial

Poly0 filling is a key step for vertical transistor integration. Poly voids may impact transistor reliability or induce word line connection issues (resistive or open contacts) (Fig.9). Several process optimizations were performed to improve poly0 filling and WL connections on trenches.

Trench aspect ratio is critical for poly0 filling. We have introduced a nitride pull back step after trench patterning to reduce nitride overhang, facilitate trench filling and to limit remaining voids (Fig.10). Combined with complementary process tuning, we successfully stabilized poly0 filling and removed all poly voids. Fig.11 compares contact resistance on trench between initial and optimized processes. Contact resistance mean values and spread are significantly improved with new processes.

IV. RESULTS

A. Select transistor characterization

Main critical point is to have a reproducible, and reliable vertical transistor MOS. Fig.12 shows single select drain current (Id) versus Gate voltage (Vg) curves for read (Vd~0.5V) and write (Vd~4V) operation conditions at 25°C and 125°C. Id(Vg) curves show standard MOS behavior with leakage current inside specification to sustain maximum bitline leakage criteria. Fig. 13 shows select transistor gate oxide lifetime extrapolation at ambient (25°C) and hot temperature (125°C) demonstrating high margin versus specification.

B. eSTM Cell characterization

Fig.14 represents single eSTM Cell Id(Vg) curves measured at 25°C and 125°C showing the window between erased and programed states. Write threshold is positive whereas erased cell is totally depleted with negative threshold. Many characterizations have been performed on eSTM to evaluate the best way to activate the cell. For instance, Fig 15 shows programing kinetic versus drain (Vd) and control gate (Vcg) voltages. Best programming efficiency is obtained for select gate bias (V_{gSEL}) near threshold voltage as shown on Fig.16. In this condition, electron current during write operation is minimized and cell consumption is in the range of 1µA (Fig 17) which is in line with split gate consumption reported in literature [8].

Strong reliability and high cycling capability are required for embedded NVM in advanced product. Fig.18 represents the programming window evolution during cycling from 0 to 500kCycles. Threshold voltage degradation occurs only on Erase state and it is compensated at product level thanks to an adaptive algorithm on CG voltage during erase operation.

V. CONCLUSION

In this paper we disclosed the eSTM NVM cell developed to address microcontroller markets. Tens of millions units have been produced on 40nm node. This cell shows a very compact footprint with a bitcell area of 0.049µm^2. It's claimed to be the smallest 40nm charge storage based NVM on the market, and should remain competitive compare to several 28nm conventional charge storage cells [9-11].

Scalability is supported by a simple cell architecture having only one contact per cell. On other hand, reduced drain-source voltage facilitates further reduction of storage MOS length. A shrunk version is currently under development for next microcontroller product generation.

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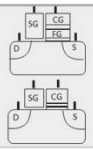
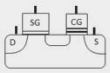
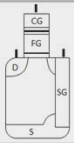
Cell Architecture	1T eFlash Planar	1.5T Split-gate Planar	2T UCP Flash Planar	1.5T eSTM Vertical
Device Schematic				
Technology node (Prod ➔ R&D)	40nm	40 ➔ 28nm (FG) 22nm (SONOS)	40nm	40 ➔ 28nm
Memory layer	FG	FG or ONO	ONO	FG
cell Area (40nm)	0.059µm²	0.053µm²	0.079µm²	0.049µm²
P/E Mechanism	CHEI / FN	SSI / FN or SSI / HHI	FN / FN	SSI / FN
Prog. Time	~ µs	~ µs	~ ms	~ µs
Prog. Consumption	> 50µA	~ 1µA	~ pA	~ 1µA
Endurance	100K	100K-1M	100K	100K-1M
Scalability	-	+	- -	+ +
Process complexity	Low	Medium (ONO) – High (FG)	Low	Medium
Applications	Auto / GP / SC	Auto / GP / SC	SC	Auto / GP / SC

Table I. 40nm cell architecture benchmark (CHEI stands for Channel Hot Electron Injection and HHI for Hot Hole Injection).

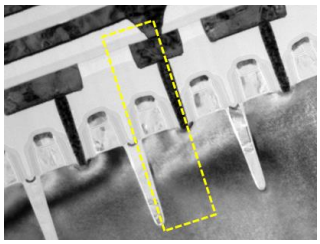


Fig.1. eSTM cell Transmission Electron Microscopy (TEM) cross section. Doted line highlight one bitcell.

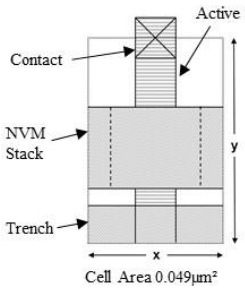


Fig.2. eSTM cell layout.

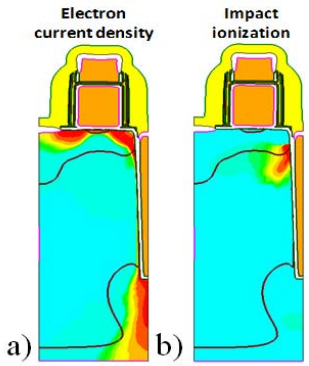


Fig. 3. TCAD simulations of (a) electron current density and (b) impact ionization during programming operation.

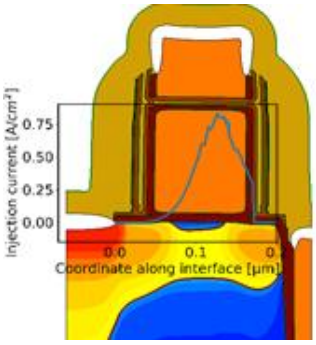


Fig. 4. TCAD simulation of injection current distribution along tunnel oxide interface during programming.

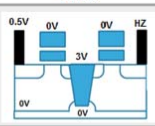
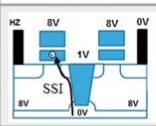
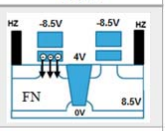
Operation	Read	Write	Erase
Schematic			
Bit-Line (BL)	~0.5V	~4V	Hz
CG line	0V	~8V	~-8.5V
Word Line (WL)	~3V	~1V	4V
Source	0V	0V	~8.5V
Pwell	0V	0V	~8.5V

Table II. eSTM cell activation conditions description.

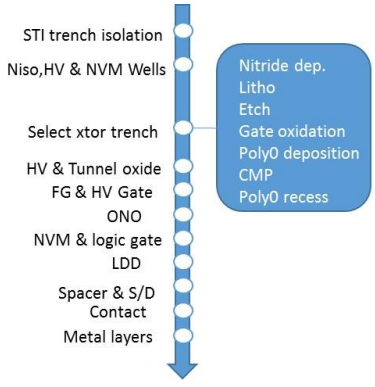


Fig. 5. Process flow description.

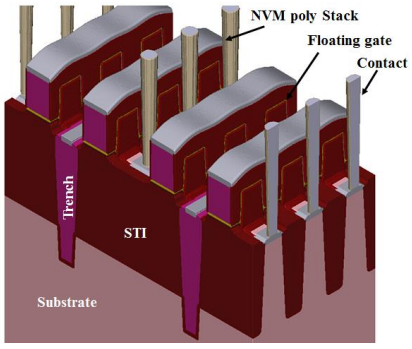


Fig.6. eSTM cell 3D view.

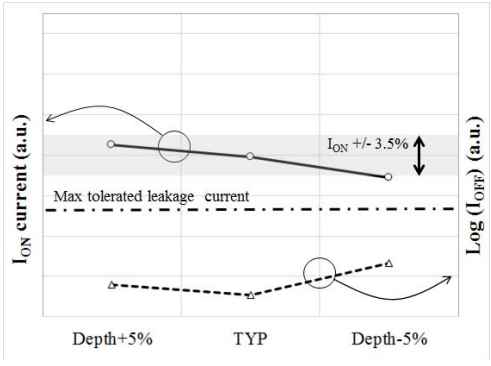


Fig. 7. vertical select transistor parameters (I_{ON} & I_{OFF}) versus trench depth.

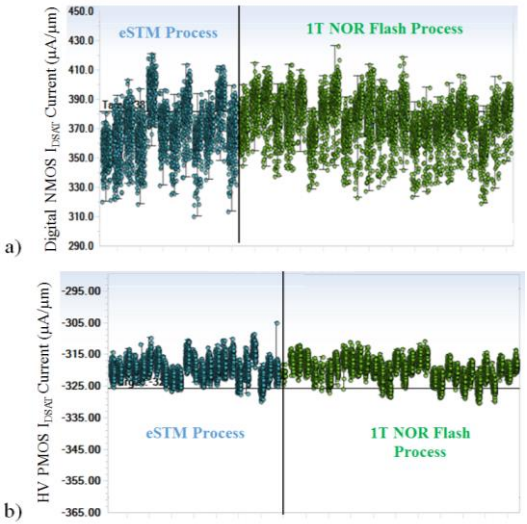


Fig. 8. Digital & HV MOS parametric (saturation current) trend on around 1000 wafers showing good alignement between 1T NOR and eSTM process flow.

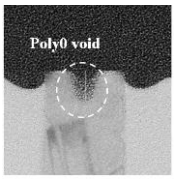


Fig.9. Poly0 void TEM cross-section

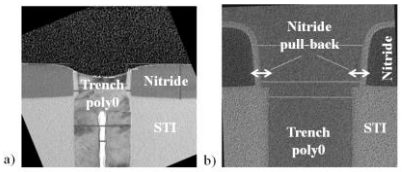


Fig.10. TEM cross-section (a) without and (b) with nitride pull-back process.

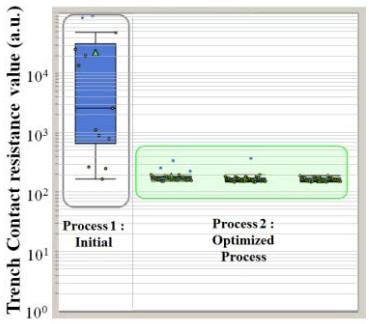


Fig.11. Voids impact on trench contact resistance with initial and optimized process.

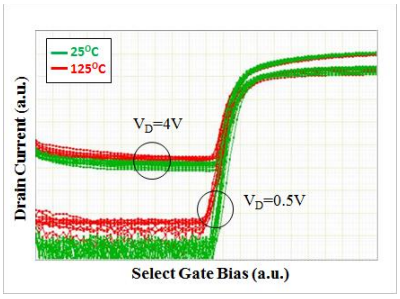


Fig. 12. Select transistor Id(Vg) curves for both read (Vd~0.5V) and write (Vd~4V) conditions at ambient (25°C) and hot temperature (125°C).

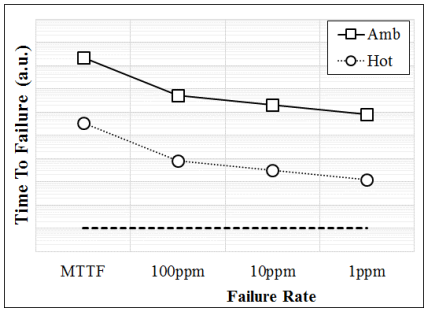


Fig. 13: Select transistor gate oxide lifetime extrapolation at ambient(25°C) and hot temperature (125°C) showing high margin versus specification.

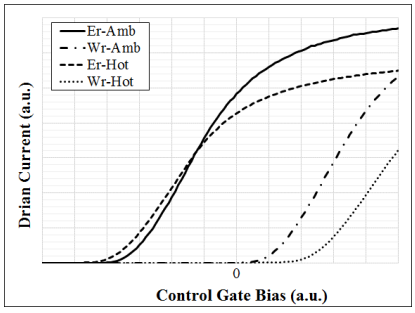


Fig.14. eSTM Cell Id(Vg) curves in both write and erase states at ambient (25°C) and hot temperature (125°C). Erase state threshold is negative.

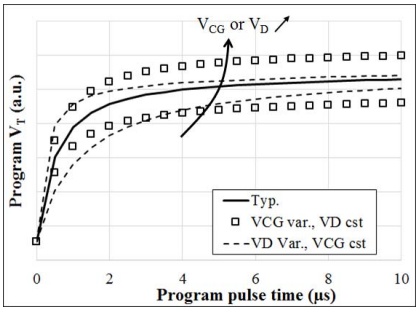


Fig.15. eSTM V_T kinetic during programming operation with typical conditions and V_{CG}, V_D bias variations.

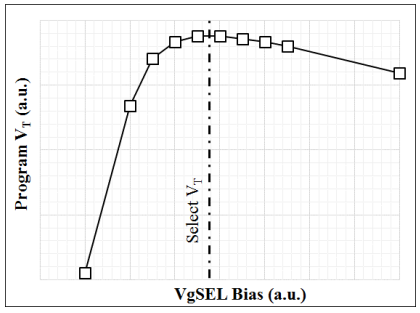


Fig.16. eSTM Write threshold voltage versusV_{gSEL} bias :optimum V_T Write obtained for V_{gSEL} bias around select threshold.

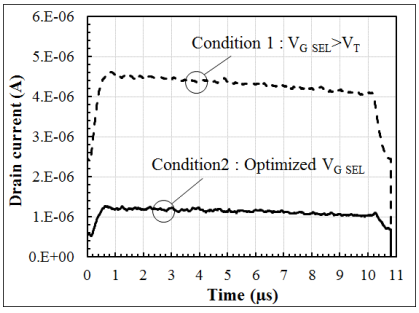


Fig. 17. Dynamic drain current measured during programing step: current consumption peak is in the range of 1µA.

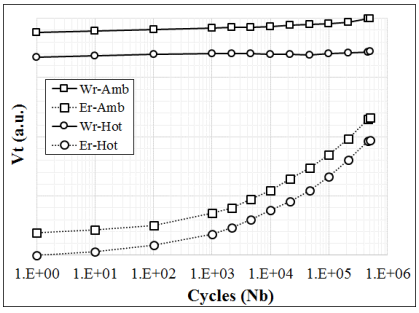


Fig.18. eSTM single cell erase and program threshold evolution during cycling at ambiant (25°C) and hot temperature (125°C).