40nm embedded Select in Trench Memory (eSTM) Technology Overview

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Abstract— **The eSTM (embedded Select in Trench Memory) is a floating gate based non-volatile memory cell conceived, developed and industrialized by STMicroelectronics for General Purpose and Secure Microcontrollers embedded applications. Thanks to its unique architecture, the eSTM cell gathers the advantages of a conventional split-gate NVM cell together with a more compact cellbit area than a typical 1T Flash Memory cell, and it is claimed to represent the scalability limit for a floating gate based NOR NVM.**

Index terms— Nonvolatile memory, embedded, trench, vertical transistor, Source Side Injection

I. INTRODUCTION

Today, Semiconductor Companies and Foundries are deeply engaged in the process of development and manufacturability demonstration of the next generation advanced solutions for embedded NVMs (MRAM, PCM, RRAM etc.). In the meantime, conventional charge storage based NVMs maintain the lion's share of the market, pushing the manufacturers to pursue the efforts in floating gate and MONOS cells scaling. In this scenario, STMicroelectronics has developed an innovative solution allowing to achieve a breakthrough scaling of a floating gate based NVM cell.

II. CELL DESCRIPTION

The eSTM cell consists of a storage element structured as a conventional stack of a polysilicon floating gate (FG) and a polysilicon Control Gate (CG), and a select transistor (wordline) which is built vertically in the depth of the silicon, reaching an n-buried diffusion (n-iso) as depicted in **Fig.1**.

The eSTM cell layout is described in **Fig.2**; the cell version which is actually manufactured and commercialized by STMicroelectronics has a bitcell area of $0.049\mu^2$, making eSTM the smallest 40nm charge storage based NVM on the market **[1]**, and even smaller than other 28nm conventional charge storage based NVM cells **[2]**.

The n-iso diffusion, together with an n-well diffusion surrounding the memory array, plays the role of common source line, also allowing the isolation of the array p-well with respect to the p-type silicon substrate. A suitable n-type doping of the storage element channel makes the cell conductive when it's in the virgin state (normally on) **[3]**.

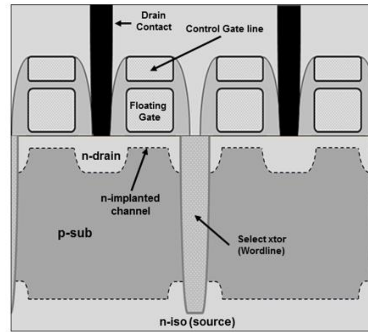

Fig.1. .Schematic cross-section of eSTM cell.

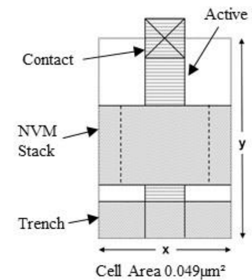

Fig.2. eSTM cell layout.

The structure of the vertical select transistor determines the simultaneous selection of the two rows of cells symmetrically placed with respect to the vertical trasistors itself (twin cells). The unambiguous selection of one single memory cell among the twin is granted by the connection of each drain to one of two different metal bitline (double bitline), as shown in **Fig.3**.

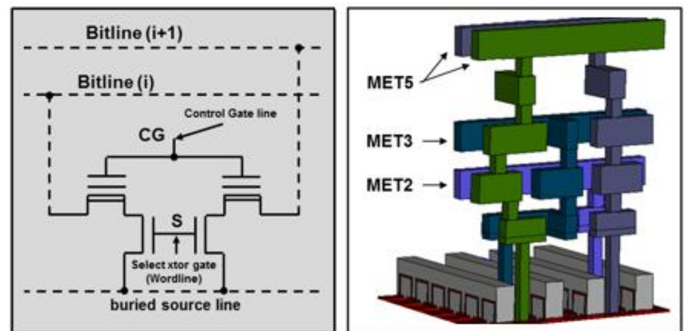

Fig.3. Device schematic of coupled cells arrangement (left) and Back-end interconnection illustration of 4 bitlines (right).

The problem of the connection of the cells, placed on the same vertical pitch, alternatively to two different bitline, without impacting the optimum cell footprint, has been solved through a smart back-end routing **[4]**; four bitlines are drawn in the equivalent X pitch of 2 cells, allowing to reach a BE connection compatible with the optimized cell width. In a preferred arrangement of the memory array, the Control Gate lines of cells twins are connected together. A memory page is then composed by the plurality of cells belonging to 2 CG lines and selected by the same wordline.

III. PROCESS INTEGRATION

The eSTM specific trench definition steps are performed at the beginning of the flow. Active, Niso, HV and NVM well implants are defined similarly to a 1T NOR flash cell. Select Trench steps are then inserted in the flow prior to the HV & Tunnel oxide definition as shown on **Fig.4**. The trench patterning and poly filling as illustrated on **Fig5**. represent the key challenge for this cell integration in particular to maintain manufacturing compatibility with all others devices on this technology platform **[5]**.

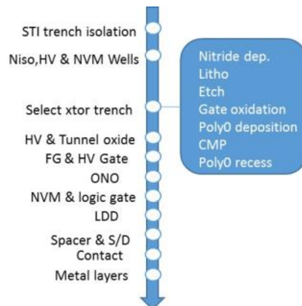

Fig.4. Process flow description.

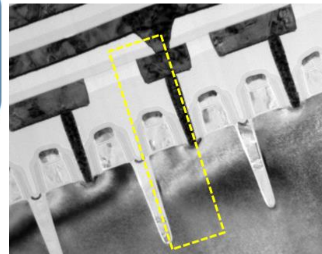

Fig5. eSTM cell TEM cross section. Dotted line highlights one bitcell

IV. CELL OPERATIONS

In cell reading operation, a voltage of about 0.7V is applied by the sense amplifier to the selected bitline while the selected wordline is biased around 3V. The Control Gate line is kept at GND potential. Source line is grounded, as well as the array p-well. Typical read biasing condition are pictured in **Fig. 6**.

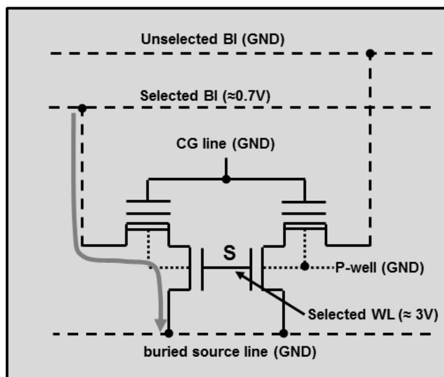

Fig.6. Device schematic and bias during read operation.

Erased cell is characterized by significant negative threshold voltage while programmed cell has positive threshold voltage. Typical read characteristics of erased and programmed cells are shown in **Fig.7.**

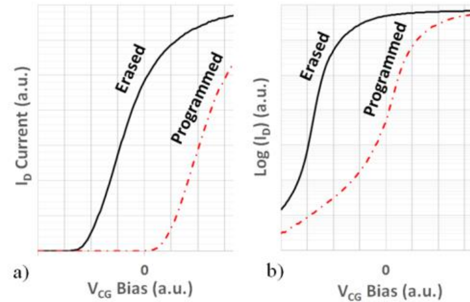

Fig.7. Measured I_D-V_{CG} characteristics of erased and programmed eSTM cell. (a) Linear scale and (b) logarithm scale.

The cell erase operation is performed on a whole page through FN tunneling mechanism; typical page size is 512Bytes. Biasing conditions for cell erase operation are described in **Fig.8.**

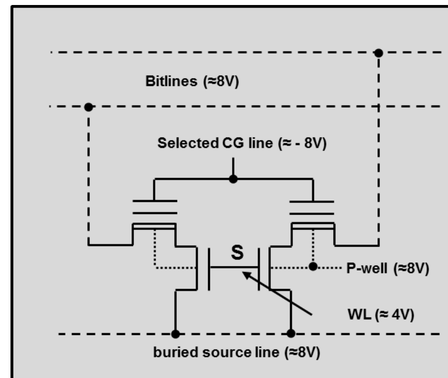

Fig.8. Device schematic and bias during FN erase operation.

The array p-well and the bitlines, together with the n-iso region are biased to a high positive voltage (e.g. +8V). The selected CG line is forced to a high negative voltage (e.g. -8V). The wordilines do not play any role during erase operation, and they are biased to a moderate positive voltage (e.g. 4V) in order to minimize the gate oxide electric stress vs. the p-well. The unselected CG lines are biased at the same positive voltage of the p-well, so that no electrical disturb is seen by unselected pages during page erase. The capability of the CG decoder to manage simultaneously high positive and negative voltage is granted thanks to a specific architecture based on isolated p and n wells. This has been achieved within a modest silicon area, thanks to the small dimension of the used HV MOS transistors, since CG decoding is not required in read operation. Alternatively to page erase capability, CG decoder can be arranged in order to provide sector erase capability (typically 4-8Kbytes sectors). This choice allows further layout size reduction of the CG decoder. Erase time for a page or a sector is < 2ms; faster erase time compared to conventional split-gate cells **[6] [7]** represent a major advantage in application requiring aggressive transaction time (Secure Microcontrollers).

For bit programming operation, the wordline is biased at a voltage of about 1V (slightly above the vertical MOS

threshold voltage). The bitline connected to the drain of the cell to be programmed is biased around 4.5V. The Control Gate line is biased with a high voltage level in the range of 8V. The buried source line and the p-well remains at GND. Thanks to the high voltage applied to the Control Gate line, the voltage applied to the drain of the cell is fully transferred to the source of the storage element which also represents the drain of the vertical select transistor. It follows that the vertical select transistor is biased in a saturation condition with a V_{DS} voltage of 4.5V; such a condition determines the generation of hot electrons in the vertical MOS drain region, in proximity of the source of the storage element. The vertical electric field controls the hot electron injection mechanism in the floating gate (SSI). The programming current can be controlled by wordline voltage, which is generated through a current mirroring principle based on the select transistor of a reference cell **[8]**.

A schematic description of the bit program operation and the circuit for the generation of the wordline voltage during the programming operation is shown in **Fig.9**.

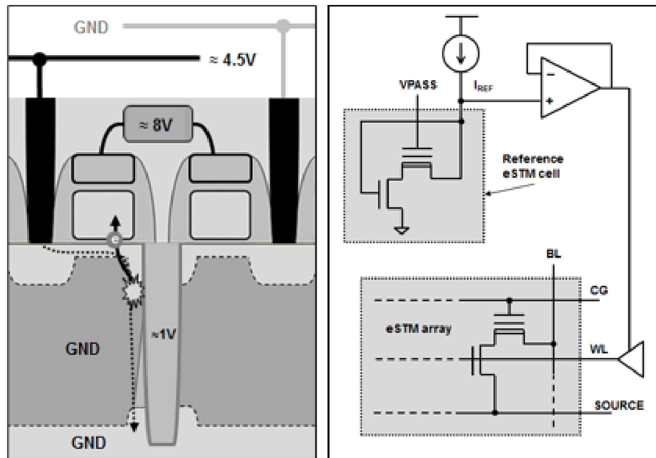

Fig.9. Schematic cross-section with SSI mechanism principle during program operation (left) and wordline biasing generator for eSTM cell programming operation (right).

A programming reference current is injected in the reference select transistor, which is biased with $V_{GS} = V_{DS}$, in order to prevent from reference vertical transistor degradation; it follows that the current flowing in the cell of the array during program operation is higher than the current provided to the reference circuit due to the higher V_{DS} value. Characterizations show that the typical current flowing in the cell during programming is about 2 times the programming reference current. The eSTM cell can be programmed in 2-3 μsec with a cell programming current of 1μA, showing a programming efficiency which is comparable with a conventional split-gate cell **[9]**.

V. MACRO ARCHITECTURE

Simplified block scheme of eSTM macro architecture is shown in **Fig.10**.

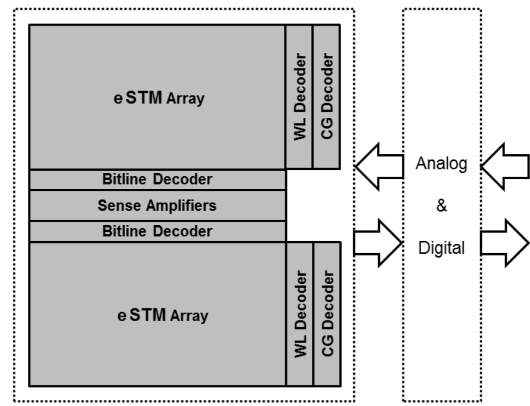

Fig. 10. eSTM macro simplified block scheme

The wordline decoder can be based on medium voltage transistors thanks to the limited voltage level to be managed during read operation (< 3.6V). During erase operation, all the wordlines are put simultaneously at high level which allows achieving higher voltage level by using n-MOS in triple well. The bitline decoder is made with special medium voltage n-MOS pass gates that are placed at edge the memory array, within the array p-well. Those choices bring a major advantage with respect to a conventional 1T NOR Flash, allowing to achieve relevant read performances, either in terms of speed or for dynamic consumption reduction.

TABLE I summarizes the key design specification of an eSTM macro for a General Purpose microcontroller without algorithm assisted write operations, while TABLE II refers to the specifications of a macro for a Secure application, embedding program/erase algorithm.

CMOS Process	40nm
Memory Density	1Mbyte
Dual Power Supply	0.85V ÷ 1.35V & 1.6V ÷ 3.6V
Operating Temperature (Tj)	-40°C to 135°C
Sector	8KBytes
Output Data Bus Width	128 Bits
Access time	< 20ns (1.05V ÷ 1.35V) < 40ns (0.85V ÷ 1.05V)
Idle consumption	< 10μA
Read Dynamic Consumption	<150μA/MHz
Error Correction Code	SEC/DED
Algorithm Assisted Write	No
Write Troughput	1Mbytes/sec
Sector Erase Time	<2ms
Mass Erase Time (1Mbyte)	<5ms
Write Endurance	10Kcycles

Table I: Target specifications for General Purpose microcontroller

CMOS Process	40nm
Memory Density	2Mbytes
Dual Power Supply	0.9V ÷ 1.4V & 1.6V ÷ 5V
Operating Temperature (Tj)	-40°C to 125°C
Page/Block	512Bytes/2KBytes
Output Data Bus Width	64 Bits
Access time	< 25ns (1.05V ÷ 1.4V) < 60ns (0.9V ÷ 1.05V)
Idle consumption	< 200μA
Read Dynamic Consumption	<160μA/MHz
Error Correction Code	SEC/DED
Algorithm Assisted Write	Yes
Page programming time (typ)	800μsec
Page Erase Time	<0.9ms
Block Erase Time	<1ms
Write Endurance	500Kcycles

Table II: Target specifications for Secure microcontroller

VI. ENDURANCE

Erase and program operation can be performed as elementary operations if cycling requirement remains in the range of few tens of Kcycles. The cycling capability can be extended to 500 Kcycles and above through the introduction of algorithm assisted operations. **Fig.11** and **Fig.12** show the comparison of erased and programmed cells distributions measured on fresh array and after 10Kcycles without algorithm or after 500Kcycles assisted by embedded algorithms respectively.

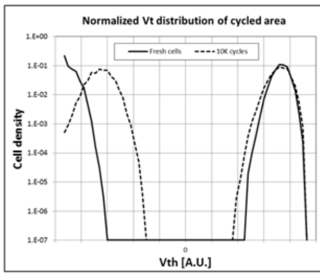

Fig.11. Cells V_T distributions before and after 10K cycles without algorithm (at room temp.)

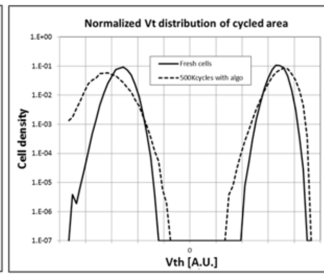

Fig.12. Cells V_T distributions before and after 500K cycles with algorithm (at room temp.)

The only relevant cumulative disturb mechanism on unselected pages/sectors during cycling is represented by the drain stress generated during programming. Drain stress acts both on erased and programmed cells, and it is function of cell aging and unselected CG lines biasing voltage. **Fig.13** shows the effect of disturb due to equivalent drain stress of 500Kcycles on erased and programmed cells, either on fresh cell or on cell cycled 500K times, vs. unselected CG line voltage.

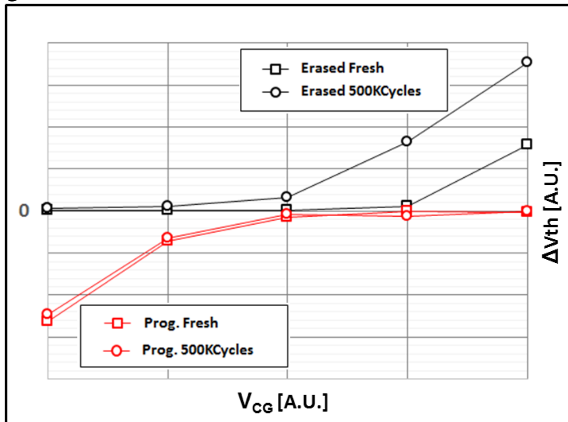

Fig.13. Cell threshold voltage drift evolution after drain disturb on erased and programmed cells.

Unselected CG lines can be biased at a voltage level making drain stress effective on programmed cells only; such a disturb can be managed by the internal write algorithm.
Effect of drain disturb on cell distributions is shown in **Fig.14** and **Fig.15**.

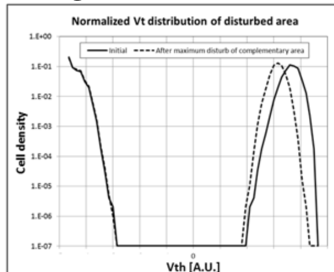

Fig.14. Cells V_T distributions before and after 10K cycles cumulative drain disturb (without algorithm and at room temp.)

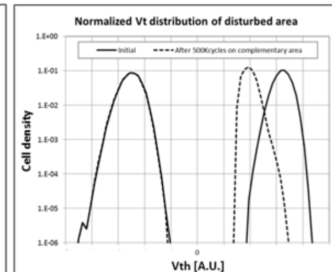

Fig.15. Cells V_T distributions before and after 500K cycles cumulative drain disturb (with algorithm and at room temp.)

VII. CONCLUSIONS

This document discloses the eSTM Flash Memory cell that has been conceived, developed and industrialized by STMicroelectronics. Secure and General Purpose microcontrollers embedding eSTM are already present on the field or they are in the qualification phase. **Fig.16** shows a die photograph of a microcontroller of the STM32 family produced by STMicroelectronics; this device, processed in 40nm technology, embeds two eSTM memories of 1Mbyte each, including SEC/DED correction code.

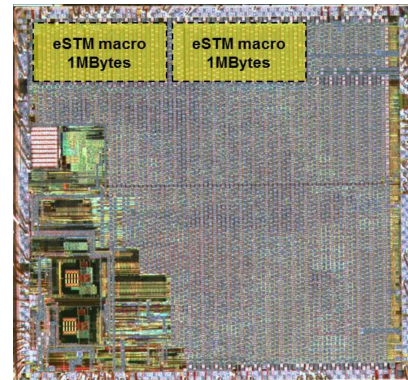

Fig.16. Snapshot of STM32 microcontroller by STMicroelectronics embedding two 1MBytes eSTM macros in 40nm technology.

In the light of the performances, the reliability, the endurance and the inherent robustness to operating stresses, eSTM cell aims to be the 40nm best-in-class solution in the domain of the commercial embedded charge storage non-volatile memories.

REFERENCES

[1] J. Pak et al., “40nm & 22nm Embedded Charge Trap Flash for Automotive Applications”, IMW, p121-124, 2018

[2] Y. Taito et al., “A 28nm Embedded Split-Gate MONOS (SG-MONOS) Flash Macro for Automotive Achieving 6.4GB/s Read Throughput by 200 MHz No-Wait Read Operation and 2.0 MB/s Write Throughput at Tj of 170°C”, IEEE JSSC, VOL. 51, NO. 1, Jan 2016

[3] F. La Rosa, S. Niel, A. Regnier, “Read performance of a non-volatile memory device, in particular a non- volatile memory device with buried select transistor”. US Patent No 9825186 (2017, Nov)

[4] F. La Rosa, S. Niel, A. Regnier, “Twin memory cell interconnection structure”. US Patent No 9941012 (2018, Apr)

[5] S. Niel et al, “Embedded Select in Trench Memory (eSTM), best in class 40nm floating gate based cell: a process integration challenge”, IEDM, 2018

[6] L. Q. Luo et al., “40nm Embedded Self-Aligned Split-Gate Flash Technology for High-Density Automotive Microcontrollers” IMW, p123-126, 2017

[7] L. Q. Luo et al., “Functionality Demonstration of a High-Density 2.5V Self-Aligned Split-Gate NVM Cell Embedded Into 40nm Logic Process for Automotive Microcontrollers”, IMW, p149-152, 2016

[8] F. La Rosa, S. Niel, A. Regnier, J. Delalleau, “Hot-carrier injection programmable memory and method of programming such a memory”. US Patent No 9224482 (2015, Dec)

[9] Y. Tkachev et al., “A Detailed Analysis of Hot-Electron Programming Efficiency in 40-nm Split-Gate Flash Memory Cell”, IMW, p48-51, 2017